CHIP SPECIFICATION

TCC8801

High Performance and Low-Power Processor

For Digital Media Applications

Rev. 1.02

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TelcChips

Revision History

Date	Revision	Description
2010-07-19	1.00	∗ Initial release
2010-11-12	1.01	∗ Correct the document format.
2011-01-28	1.02	∗ Correct the register table.
2011-03-05	1.02	* GPIOF port multiplexing (Table 3.7 Function 7). * Update pin description. * Ball number fix GPIOA[14] F10->E10 (Table3.2). * Add GPIO Initial Status (Table3.x). * Add limitation of SD Port3 usage(Table3.7).

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1 Introduction

For new, innovative user experience by PC-like web browsing, Full HD video, intuitive user interfaces, location based services, and next generation social networking applications, Telechips presents the TCC8801 multimedia application processor. The TCC8800F is built and optimized for Smart Phone, Feature Phone, PMP, Mobile TV, Portable Navigation, Set-top box, and more.

TCC8801 integrates the ARM® Cortex-A8 microprocessor core with 256KB unified L2 cache, and hardwired VPU/GPU/ISP to maximize multimedia experience at its peak level. The hardwired VPU enables 1080p full HD video encoding and decoding, and the GPU offers up to 20M polygon 3D graphic with OpenGL ES2.0 and Open VG 1.1. The ISP provides AWB, AE Control, Auto Focus, Lens Shade Corrector, Bad Pixel Correction, WDR, and etc. It can support various bases of operation systems such as Linux®, Android, and Windows® CE.

The TCC8801 is a great processor for networked devices which require the ease of connectivity functions: The USB OTG and USB OTG Host controllers will enable the data transmission between the multimedia device and storage devices. The Ethernet MAC controller provides internet connection, compliant to IEEE802.3 standard. The SATA controller powers the multimedia device to connect with HDD.

This innovative and rich feature set will expand the categories of applications yet to be imagined.

1.1 TCC8801 Features

Table 1.1 TCC8801 Features

Category	Description
PROCESSORS (CORTEX-A8)	• In-order, dual-issue, superscalar microprocessor core - 13-stage main integer pipeline - 10-stage NEON media pipeline - Dedicated L2 cache with programmable wait states - Global history based branch prediction • Works in conjunction with a power optimized load store pipeline to deliver 2.0 DMIPS/MHz for power sensitive applications • ARMv7 architecture compliant including - Thumb®-2 technology for greater performance, energy efficiency, and code density - NEON™ signal processing extensions to accelerate media codecs - Jazelle RCT Java-acceleration technology - TrustZone technology for secure transactions and DRM • Integrated 256KB Unified Level 2 Cache • Optimized Level 1 Cache (Code:32KB, Data:32KB) • Dynamic Branch Prediction • Memory System - Single-cycle load-use penalty for access to the L1 cache - Hash array in the L1 cache limits activation of the memories to when they are likely to be needed - Direct interface between the integrated, configurable L2 cache and the NEON media unit for data streaming - Banked L2 cache design that enables only one bank at a time - Support for multiple outstanding transactions to the L3 memory to fully utilize the CPU • JTAG debug interface and ETM Trace Port
MEMORY ORGANIZATION	• **Internal(On-Chip) Memory** - 32KB Boot-ROM (EHI, NAND, USB Boot with security and etc.) - 80 KB Internal SRAM • **External(Off-Chip) Memory**[1] - LPDDR SDRAM : up to 200MHz(400Mbps) - LPDDR2 SDRAM : up to 400MHz(800Mbps) - DDR2 SDRAM : up to 400MHz(800Mbps) - DDR3 SDRAM : up to 400MHz(800Mbps) - LPDDR/LPDDR2/DDR2 SDRAM : Support 16/32 bit data bus - DDR3 SDRAM : Support 32 bit data bus
VIDEO CODEC	▪ **Decompressor**[2] **(Decoder) – up to 30fps @ Full-HD (1920x1080)** • H.263 - Up to Baseline Profile + AnnexI,J,K(RS=0 and ASO =0),T - Including Sorenson Spark - Max. bitrate : up to 30Mbps • MPEG 1/2 - Up to Main Profile @ High Level - Max. bitrate : up to 80Mbps • MPEG4-ASP - Up to Advanced Simple Profile Including DivX 3.x/4.x/5.x/6.x - Max. bitrate : up to 35Mbps • MPEG4-AVC(H.264) - Up to High Profile @ Level 5.1 - Max. bitrate : up to 40Mbps • VC-1 - Up to Advanced Profile @ Level 3.0 - Max. bitrate : up to 45Mbps

[1] The maximum memory clock is dependent on the operation voltage. Refer to Electrical specification
[2] The performance of the video decoding can be limited by the overall system bus traffic

	• RV - Real Video 10 (Backward Compatible for RV 8/9) - Max. bitrate : up to 30Mbps • AVS - Jizhun Profile @ L6.2 - Max. bitrate : up to 40Mbps • MJPEG/JPEG - Up to 32M pixel/s - Max Image Size : 8192 x 8192 ▪ **Compressor[3] (Encoder) – up to 24fps ~ 30 fps @FHD(1920x1080)** • H.263 : up to 30fps @ FHD(1920x1080p) • MPEG4-ASP : up to 30fps @ FHD(1920x1080p) • H.264 : up to 24fps ~ 30 fps @ FHD(1920x1080p) • MJPEG/JPEG : up to 32M pixel/s (Max 4096x4096)
GRAPHIC ENGINE	▪ **2D/3D Graphic** • High Geometry and Pixel Processing • Up to 20M polygon[4] • Full OpenVG v1.1 Support - Lines, Squares, Triangles, Points - Vector Graphics - ROP 3/4 - Arbitrary Rotation / Scaling - Alpha Blending - Multitexture BItBLT • Full OpenGL ES v2.0, v1.x Support - 4X /16X FSAA - Flat/Gouraud Shading - Perspective Correct Texturing - Point Sampling/Bilinear/Trilinear Filtering - Mipmapping - Multi Texturing - Dot3 Bump Mapping - Alpha Blending - Stencil Buffering (4-bit) - JSR 184 - Point Sprites - 2 bit per pixel Texture Compressing (FLXTC) - 4 bit per pixel Texture Compressing (ETC) ▪ **Overlay Mixer** – 8bpp (RGB332) – RGB (444, 454, 555, 565, 666, 888) – Alpha-RGB (444, 454, 555, 666, 888) – Sequential YUV (444, 422) – Separated YUV (444, 440, 422, 420, 411, 410) – Interleaved YUV (422, 420) – BitBLT (16 Raster Operations) – 3 Channel Source Mirror/Flip/90°, 180°, 270° Rotate – 1 Channel Destination Mirror/Flip/90°, 180°, 270° Rotate – 3 Channel Arithmetic Operation – 3 Channel YCbCr-to-RGB Color Space Converting – Overlay and Alphablending (2 overlay, 256-level alphablending) – Color LUT – Dithering
IMAGE ENHANCEMENT	• **Histogram Measurement** - Analyze the Luminance Components - Multi-frames Average Mode - User-defined Pixel Segments Support

[3] The performance of the video encoding can be limited by the overall system bus traffic
[4] The performance of the polygon processing can be limited by the overall system bus traffic

	• **Contrast Enhancement** - User-defined Scaling Segments - Multi-frames Average Mode • **De-Interlacer** - Motion-adaptive and Pixel-based Processing - Film-mode Detection - Simple Edge-oriented Mode - Advanced Spatial-Temporal Mode • **Noise Reduction** - Directional-Smoothing Filter - Temporal-Recursive Filter - Noise Estimation • **Sharpness** - Spatial High-pass Filter
DISPLAY INTERFACE	▪ **Display Controller** • 2 Display Controllers - Controller 0 has 4 image channels - Controller 1 has 4 image channels - Progressive or Interlaced Digital Video Output - 4 Channel Overlay / Chroma-Keying / Alpha-blending - Gamma Correction - Look-up table for Indexed or RGB Color - Contrast, Brightness, Hue Function Supported. ▪ **Supported Output Media** - TFT-LCD - HDMI Output : up to 1920x1080p - Composite TV-Out (NTSC/PAL) : NTSC(720x480), PAL(720x576) - LVDS Output - MIPI DSI ▪ **Dual-Display Supported**[5] - Two types of supported media - CPU Type Main/Sub LCD : Time Shared
CAMERA INTERFACE	•* **Camera I/F (parallel)** - CCIR-601/656 Interface - Camera Input Supported - 1 Channel Overlay / Chroma-Keying - Image Effect(Gray/Negative/Sepia/Emboss/Sketch & ETC.) - Up-scaling (x4), Down-scaling(x1/1024: X/32, Y/32) • **Image Signal Processing (ISP)** - Bad pixel detection and correction - Lens shade correction, separate for R, G and B - Auto focus measurement - Auto white balancing - CAC feature - Auto exposure support by brightness measurement - Histogram calculation - Black level compensation - Enhanced color interpolation (RGB Bayer demosaicing) - Sharpening / blurring / noise filter - Color correction matrix (cross talk matrix) • **MIPI CSI 4-lane**

[5] The maximum resolution and combination of image channels can be determined by the the overall system bus traffic

TOUCH ADC	• **Touch Screen Interface** - 10/12 bits 16CH ADC - Dedicated 4 ch analog input for touch screen I/F - Shared 12 Channel analog input for general purpose[6]
AUDIO	• **Dual-I2S Master & Slave Interface** - Simultaneous 7.1 Channel & 2 Stereo channel supported • **SPDIF Transmitter/Receiver** - 5.1 Channel Supported - Support Tx 2 Channel or Tx 1 Channel and SPDIF Rx 1Channel • **CD I/F** - I2S Slave Interface - Up to 2 Channel
STORAGE INTERFACE	• **NAND Flash Interface** - 8 Bits / 16 Bits / 32 bits - Support 4 CS I/F - • **SD/MMC Controller** - SD, MMC/eMMC, SDIO - Up to 4 Channels (4 independent SD/MMC controller) • **Memory Stick Pro/Pro-HG Supported** • **S-ATA Interface (2ch Host or Device)** · **S-ATA AHCI** - Generation 1 : 1.5Gbps - Generation 2 : 3.0Gbps (TBD) · **S-ATA Device** - Generation 1 : 1.5Gbps - Generation 2 : 3.0Gbps (TBD)
HOST INTERFACE	• **EHI(External Host Interface)** - 8, 16bits, 18bits - 2 Channels - Bypass to LCD Port (CPU Type)
STREAMING INTERFACE	• **TS Interface** - 2 Channel TS serial/parallel interfaces (up to 8bit) • **TS Demux** - 128 PID filtering & Descrambling (AES, DES, MULTI2, DVB-CSA)
HIGH SPEED INTERFACE	• USB 2.0 OTG 1 Channel Interface • USB HS Host 1 Channel Interface • USB FS Host 1 Channel Interface • PCI-Express x1 Interface
NETWORK INTERFACE	• **Ethernet MAC controller** - IEEE 802.3-compliant MII/GMII - Support RGMII specification form HP/Marvell
SECURITY	• **AES** - key length 128/192/256 bit

[6] The usage of 12 ch analog inputs is restricted by the port configuration because the analog inputs are shared with digital signals

	• **DES** - single/double DES - triple DES (2 key/3 key) • **MULTI2** • **DVB-CSA**
PERIPHERALS	• **UART** - Up to 6 Channels • **I2C** - Up to 4 Channel for I2C compatible interface - Configurable master/slave • **GPSB(General Purpose Serial-Bus – Master/Slave)** - Up to 6 Channels • **Infra-Red Remote Receiver** • **PWM generator** - Up to 4 Channel • **Timers** - Four 16-bit timers, two 20-bit timers - One 32-bit timer • **General DMA controller** - 12 Channels
PMU	• **RTC** - Power-Down Mode & Auto-wakeup • **Power Gating** - Internal power island for saving the current consumption.
PROCESS	• 45nm Low-Power CMOS

1.2 Applications

Category	Description
Mobile Application Processor	• Smart-Phone Application • Support of all the Mobile / Digital broadcasting services - T-DMB/S-DMB/DVB-H/ CMMB / ATSC-MH - DVB-T / DTTB • Support of Touch Screen Controller • Low-power consumption for power-down mode
Mobile Co-processor	• Mobile-TV Solution • Mobile Multimedia Co-Processor
Portable Devices	• High quality Multimedia Player • Low cost PDA application • Multimedia Host Player
Portable Navigation	• 2D/3D Navigation • Navigation with A/V System and D-TV
CAR	• Car Navigator • Multimedia Play • Multimedia Host Player
TV	• IP and Cable STB

1.3 Block Diagram

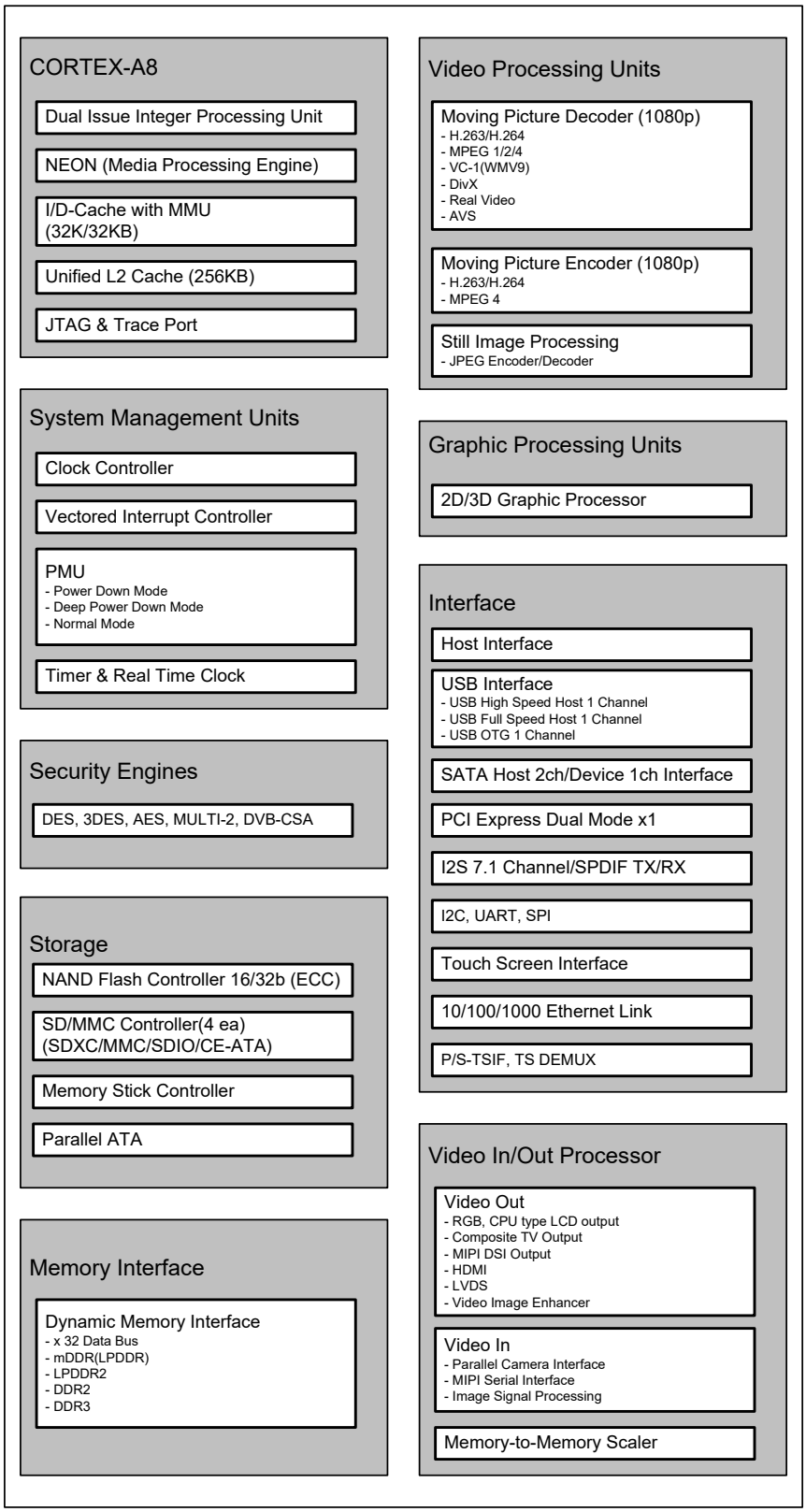


Figure 1.1 TCC8801 Functional Block Diagram

2 Hardware Features

Table 2.1 Cortex-A8 Processor

Cortex-A8	Key Features
Cache Organizations	• 32KBs/32KBs I/D L1 Caches • 256KBs Unified L2 Caches • I/D MMU Supported • Java Accelerator
Debug Interface	• JTAG

Memory Map	Description
0x00000000	• This region is remapped to as follows. 1) If Remap is 00b, On-chip Boot-ROM 2) If Remap is 01b, On-chip SRAM 3) If Remap is 10b, Off-chip DRAM 4) If Remap is 11b, Off-chip NOR .
0x10000000	Internal SRAM (80 KB)
0x20000000	MMU Virtual Table (Do not use this area)
0x30000000	Internal Boot ROM (32 KB)
0x40000000 ~ 0xBFFFFFF	External DDR SDRAM
0xF0000000 ~ 0xFFFFFFFF	Assigned to on-chip peripherals

Figure 2.1 Memory Organization

Table 2.2 Video Controller

Video Codec	Key Features
Encoder	• **H.264 Encoding** - 24 ~ 30 fps@ Full-HD Resolution (1920x1280p) • **MPEG-4-ASP Encoding** - 30fps @ Full-HD Resolution (1920x1280p) • **H.263 Encoding** - 30fps @ Full-HD Resolution (1920x1280p)
Decoder	• **H.264 Decoding** - 30fps @ Full-HD Resolution • **MPEG4-ASP Decoding** - 30fps @ Full-HD Resolution • **H.263 Decoding** - 30fps @ Full-HD Resolution • **VC-1 Decoding** - 30fps @ Full-HD Resolution • **RV Decoding** - 30fps @ Full-HD Resolution

Table 2.3 Camera Interface

CAMERA I/F	Key Features
Various Input Formats	• CCIR601/656 4:2:2 • Down Scaling for Preview Display : up to X/32, Y/32 • Change the Image size and windowing. • Support the master clock for camera module.
Camera Processing Functions	• Reconfigurable Packing the Pixel Data • Dispatching the Pixel Data into Y/Cb/Cr • Horizontal and Vertical Window Clipping • Overlaying the Background Frame for Still or Moving Pictures - Chroma-Keying - Alpha-blending (0%, 25%, 50%, 75%, 100%, XOR) • Support the Master Clock for Camera Module → w/o External Oscillator
Maximum Resolutions	• up to 120MHz[7] for Still Image[8]

7 The maximum frequency can be limited by the timing specification of the camera sensor or external device.
8 The maximum resolution can be limited by the system configuration.

Table 2.4 Video Output Interface

Video Output Interface	Key Features
Color TFT LCD	• Various type image sources - RGB565, RGB555, RGB666, RGB24, YCbCr4:2:0, YCbCr4:2:2 • Various type YCbCr4:2:0 and YCbCr4:2:2 to RGB converter • Parallel 24bits and 18bits pixel data output • 6(R):6(G):6(B)bits and 8(R):8(G):8(B)bits pixel data output
Mono/Color STN LCD	• Mono: 1, 2, 4bpp image source • Color: 8(332), 12(444), 555, 565 bpp image source • 4 and 8-bit pixel data interface
NTSC/PAL Encoder Interface	• CCIR601/656 interlace/non-interlace • RGB to YCbCr4:2:2 converter
NTSC/PAL composite output	• Supports all NTSC and PAL formats (NTSC-M/4.43, PAL-B/D/G/H/I/M/N/Combination N)
LVDS Output	• Features - Output clock range : 30M to 80MHz - 35:7 data channel compression up to 560Mpbs on each LVDS channel - Falling clock edge data strobe - 6 LVDS output channels (5 data, 1 clock channel)
HDMI Output[9]	• The supported formats are - 1920x1080p @ 60Hz - 1920x1080i @ 30Hz - 1280x720p @ 30Hz - 720x480i @ 60Hz - 720x480p @ 60Hz - etc.
Image Processing	• OSD/Overlay: can mix up to 3 image sources. - Channel 0 /Channel 1 has the 3 overlay channels. - Chroma-keying - 256 level Alpha-blending - Contrast/Brightness/Hue Control - Simple Gamma Correction Supported - LUT for each image channels • Virtual Window: Panning / Sliding the Window • Subsampling: 1/2, 1/3, 1/4, 1/8 • Duplication: x2, x3, x4, x8

9 The maximum resolution can be limited by the system configuration.

Table 2.5 DAI/CDIF Controller

I2S (DAI/CDIF)	Key Features
DAI (Digital Audio Interface)	• System clock: 256fs, 384fs, 512fs. • Maximum 7.1 channel supported • 7.1/Stereo dual-channel supported • Support of Master/Slave Mode with Reconfigurable Clock Polarity • Wide Range of Sampling Frequency in Audio application : 8kHz, 16kHz, 11.05kHz, 24kHz, 32kHz 44.1kHz, 48kHz • Supports the I2S (MSB Justified Mode) • Controls the Digital Audio Volume over the range 0dB to -90dB • Using 2 Double Buffers for Audio I/O Data
CDIF (CD Interface)	• CD Interface for Feasible Implementation of CD Application • Slave Mode • I2S (LSB Justified Mode)

Table 2.6 SPDIF Controller

SPDIF	Key Features
General Features	• Transmitter/Receiver Included • Bit Rate is 64 times the sampling frequency • Configurable 16/24 Bits Mode
Maximum Operating Frequency	• 24MHz Output Data-Rate - SPDIF Clock = 12.288MHz, Ratio = 1 - 3.072Mbps / 48kHz (Data Rate)

Table 2.7 External Device Interface

External Device Interface	Key Features
Static Memory Controller	• Support of 4 Types Static Memory (NAND/IDE/ROM/SRAM) • Controllable Setup / Pulse Width / Hold Time • 8/16 Bits Width

Table 2.8 USB 2.0 Host/OTG

USB 2.0 Host/OTG	Key Features
General Feature	• Compliant USB2.0 Specification • Support Interrupt, Bulk Transfer • Support FS/HS dual mode operation • 16bit interface • FIFO size configuration
USB DMA	• 3 Channel Scattered DMA (EP1,EP2,EP3) • Support 16/32bit MCU interface • Single / Fly mode • 4x32 FIFO for Each Endpoint
PHY Interface	• On-Chip UTMI PHY Parallel Interface
Maximum Operating Frequency	• 12 External Oscillator (Main Oscillator) • 30MHz with 16bits parallel interface

Table 2.9 Nano PHY for USB2.0 Host/OTG

UTMI PHY	Key Features
Supported Specification	• Compliant with USB 2.0 Transceiver Macrocell Interface Spec. Ver-1.04
General Features	• 480Mbps High Speed / 12Mbps Full Speed, FS Only, 1.5Mbps Low Speed • Separate 8/16 bit Unidirectional Parallel Interface • Dual-Mode Device Support (HS/FS) • Data and Clock Recovery from Serial Data on the USB Connector • SYNC/End-Of-Packet Generation and Checking • Bit Stuffing and unstuffing, Bit-stuffing Error Detection • NRZI Encoding/Decoding • Support of Suspend, Resume, Remote Wakeup Operations • Integrated HS and FS Termination and Signaling Switching • On-Chip PLL for 480Mbps • Low Power Dissipation while Active, Idle, or on Standby
System Features	• 45-ohm Termination / 1.5k Pull-up 15k Pull-down Integrated • Minimal External Components – Single Resistor
Maximum Operating Frequency	• up to 480MHz

Table 2.10 External Host Interface

EHI	Key Features
SRAM Type Interface	• 68/80 Series Interface with 8/16 Bit Width • Burst Transfer and Address Auto-Increment • Internal Interrupt Generation by an External Host Device • Semaphore Register for Improving Data Transfer Efficiency • READY can be Checked via Status Register and Pin. • LOCK MODE: External Host Device can Occupy System bus without any Handover.
Host Booting Procedure	• Configures 8/16 Bits Host Booting Mode • Host Downloads the Program into On-Chip SRAM or Off-Chip Memory • Restarts with Downloaded Program Code
Peak Access Bandwidth	• 8 Bits Configuration : 20MB/s • 16 Bits Configuration : 40MB/s

Table 2.11 SD/MMC Controller

SD/MMC	Key Features
Supported Specification	• SD ver.3.0 • SDIO ver.2.0 • eMMC ver.4.4 (Support booting from eMMC 4.4 Card)
General Features	• Automatic CRC Generation & Checking the Data/Command • Data transmit/receive FIFO (32bits x 8) • Supported SD/MMC Mode - 1 Bit Serial or 4 Bit Parallel SD - 1 Bit Serial for MMC - 4/8 Bits Parallel Transfer • External DMA Handshaking for Burst & Fast Transfer
Maximum Frequency	• up to 50MHz (TBD)[10] • Clock generation block Inside

Table 2.12 Memory Stick Controller

Memory Stick	Key Features
Supported Specifications	• Memory Stick Ver.1.x • Memory Stick Pro • Memory Stick Pro-HG
General Features	• Data transmit/receive FIFO (64bits x 4) • External DMA Handshaking for Burst & Fast Transfer
Maximum Operating Frequency	• Memory Stick serial clock (Serial : 20MHz, Parallel : 40MHz)

10 The maximum operating frequency for storage devices can be limited by the system configuration and corresponding interface ports.

Table 2.13 Nand Flash Controller

NAND I/F	Key Features
NAND I/F	• Automatic Detection of External READY Signal • Configurable Cycle Times based-on Bus Frequency • 8bit, 16bit, 32bit Interface to Buffer Memory • 16x32bits FIFO Included • External DMA Handshaking for Burst and Fast Transfer • Dedicated DMA for Burst and Fast Transfer • Dedicated MEMORY(2048Bytes) for system related data and ECC
External Configuration	• 1 NAND - Single 8 bit NAND / Single 16bit NAND • 2 NAND - Double Series 8 bit NAND / Double Series 16 Bit NAND • 4 NAND - Double Series 16 bit NAND & Quad Series 8 Bit NAND
SLC	• 2 Bit Error Detection & 1 Bit Error Correction per 256 bytes.
MLC	• 4/6/12/16/24 Bit Error Detection/Correction Based on BCH Algorithm • 8x32bits FIFO

Table 2.14 UART Interface

UART	Key Features
General Features	• 16 bytes TX/RX FIFO • Support of Hardware Flow Control (CTS/RTS) • 16 bits clock divider • 16C550 Compatible Core • Smart Card Interface
Maximum Operating Frequency	• Baud Rate Clock (3MHz ← 48MHz / 16)

Table 2.15 GPSB Interface

GPSB	Key Features
General Feature	• MSB / LSB Selection mode • Support Variable transfer (1~16bit) • Clock frequency/ Polarity selection mode • Support configurable Frame signal mode
Maximum Operating Frequency	• 60MHz for slave only • 30MHz for master mode

Table 2.16 General DMA Controller

General DMA	Key Features
General Features	• 12-Channel DMA • Dedicated Bus Interface for Various Storage Interface Controllers • Support of Byte/Half-word/Word Transfer • Support of Circular Buffer Interface - Masking of the Source/Destination Address Bits • 1/2/4/8 Burst Transfers • Byte Swapping Function • Support of Single/Continuous/Burst Mode • 8x32bits FIFO Included
DMA Request/Acknowledge	• External DMA Request/Acknowledge • Interfacing the On-chip Storage Controllers
Inter-channel Arbitration	• Configurable Priority for Each Channel • Round-robin Arbitration / Fixed Priority Arbitration

Table 2.17 Vectored Interrupt Controller

VPIC	Key Features
General Features	• 64 Individual Interrupt Sources • FIQ/IRQ Configurable • Priority Reconfigurable for Each Interrupt Sources • Polarity Controllable • Edge/Level Sensitivity Controllable • Dual/Single Edge Controllable when Edge Sensitivity Selected
Vectored Interrupt Handler	• Vector ID Returned for Fast Handling • Vector ID is one of 0 ~ 63 • 64x32 Vector Table Needed for Vector Handler on On-Chip Memory

Table 2.18 Timer

TIMER & WDT	Key Features
Timer Counters	• Four 16-bit timers with PWM output/counters, two 20-bit timers, and one 32-bit timer • External Event Counter • Stop Mode / Free Running Mode • Various Clock Sources (PLL outputs ~ Divided Sub-Clock) • PWM Functions → TREFn, TMREFn
Watchdog Timers	• Watchdog Timer Interrupt / Reset

Table 2.19 ADC

TSADC	Key Features
General Features	• 12bit Resolution • 0 ~ 3.3V Input Range (In case of 3.3V AVDD)
Operating Frequency	• 1MSPS / 5MHz
Touch Screen	• X/Y Position • Up/Down Wake-up

Table 2.20 Real Time Clock

RTC	Key Features
General Features	• Sub Oscillator Included • Clock and Calendar Function (BCD Display) - Sec/Min/Hour/Date/Day-of-Week/Month/Year • Leap Year Generation • Wakeup Signal Generation from the Deep Power-down Mode
Interrupt & Round Reset	• Alarm Interrupt in Normal Operation Mode • Cyclic interrupts 1/256, 1/64, 1/16, 1/4, 1/2, 1 second interrupts • Round-reset function 30-, 40-, 50- second
Wakeup Function	• Dedicated Wake-up Port

3 PIN Description

3.1 TCC8801 Pin Description

Table 3.1 Power/Ground Information

Group	# of Balls	Ball#	MIN(V)	TYP(V)	MAX(V)	Description
PWRCOREA	35	P17, P15, N15, N12, N11, N10, N9, P12, P11, P10, R17, R15, R14, R12, M17, M16, M15, M14, M13, M12, M11, M10, L17, L16, L13, V14, U17, U14, T17, T16, T15, T14, Y13, W12, W13	1.14	1.20	1.26	Digital Internal Core Power A
PWRCOREB	9	P13, R13, V13, V12, V11, T12, T13, U13, U12	1.14	1.20	1.26	Digital Internal Core Power B
GNDCOREAB	35	K11, K12, K13, J13, J14, J15, L11, L12, L14, L15, N13, N18, N14, N16, N17, P14, P16, R10, R11, R16, T10, T11, U15, U16, AA15, V10, V15, V16, V17, AB16, AB15, AB10, W15, U10, U11	-	-	-	Internal Core Ground (include DDR Ground)
PWRGPA	1	L9	1.71 2.38 3.14	1.8 2.5 3.3	1.89 2.62 3.46	GPIOA Group I/O Power
PWRGPB	2	M9, M8				GPIOB Group I/O Power
PWRGPC	2	V9, U9				GPIOC Group I/O Power
PWRGPD	1	J9				GPIOD Group I/O Power
PWRGPDH	1	J10				GPIODH Group I/O Power
PWRGPE	1	W8				GPIOE Group I/O Power
PWRGPF	1	M7				GPIOF Group I/O Power
PWRGPG	2	U8, U7				GPIOG Group I/O Power
PWRETC	1	K22				ETC Group I/O Power
GNDGPA	1	J8	-	-	-	GPIOA Group I/O Ground
GNDGPB	2	K8, J7	-	-	-	GPIOB Group I/O Ground
GNDGPC	2	N7, P8	-	-	-	GPIOC Group I/O Ground
GNDGPD	1	K9	-	-	-	GPIOD Group I/O Ground
GNDGPDH	1	K10	-	-	-	GPIODH Group I/O Ground
GNDGPE	1	P9	-	-	-	GPIOE Group I/O Ground
GNDGPF	1	N8	-	-	-	GPIOF Group I/O Ground
GNDGPG	2	T8, R9	-	-	-	GPIOG Group I/O Ground
GNDETC	2	AA17	-	-	-	ETC Group I/O Ground
PWRMEMQ	9	AA13, AA14, AB13, AB14, Y14, Y15, Y16, W14, W16	1.2		1.8	DDR/mDDR I/O Power
PWRMEMZQ	1	W9				DDR ZQ Calibration Power
PWRMEMCKE	1	Y12				DDR CKE Power
GNDMEMZQ	1	T9	-	-	-	DDR ZQ Calibration Ground
GNDMEMCKE	1	AC13	-	-	-	DDR CKE Ground
PWRHDMIOSC	1	H12	3.14	3.3	3.46	HDMI OSC Power
PWRHDMI12A	1	F13	1.14	1.20	1.26	HDMI Power
PWRHDMIPLL	1	G12	1.14	1.20	1.26	HDMI PLL Power
GNDHDMIOSC	1	L10	-	-	-	HDMI OSC Ground
GNDHDMI12A	2	H13, G13	-	-	-	HDMI Ground
PWRMIPIPLL		F16	1.14	1.20	1.26	MIPI PLL Power
PWRMIPI18D		J17	1.71	1.8	1.89	MIPI 1.8 Power
PWRMIPI12D	5	H16, K16, K14, J16, K15	1.14	1.20	1.26	MIPI 1.2 Power
GNDMIPI	5	H14, G14, G15, G16, H15	-	-	-	MIPI Ground
PWROSC	1	J23	1.71	1.8	1.89	Oscillator Power
GNDOSC		N21	-	-	-	Oscillator Ground
PWRPLL0	1	M21	1.14	1.20	1.26	PLL0/4/5 Power (High freq PLL)
PWRPLL1	1	L20	1.14	1.20	1.26	PLL1/2/3 Power (Low freq PLL)
GNDPLL	2	P20, P19	-	-	-	PLL Ground
PWRRTC	1	M23	1.5	3.0	3.3	RTC Core & I/O Power
PWRADC	1	H17	2.7	3.3	3.6	ADC Power
ADC_VREF	1	G26	2.7	3.3	3.6	ADC Reference Voltage
GNDADC	2	M18, N19	-	-	-	ADC Ground
PWRDDAC	1	W20	2.7	3.0	3.3	DAC Digital Power
PWRADAC	1	V18	2.7	3.0	3.3	DAC Analog Power
GNDDDAC	1	Y17	-	-	-	DAC Digital Ground
GNDADAC	1	U19	-	-	-	DAC Analog Ground
PWRLVDS33A	1	F19	2.7	3.3	3.6	LVDS 3.3V Power
PWRLVDS12A	1	G17	1.14	1.20	1.26	LVDS 1.2V Power
GNDLVDS33A	2	P18, K20	-	-	-	LVDS 3.3V Ground
GNDLVDS12A	1	N20	-	-	-	LVDS 1.2V Ground
PWRSATA0	1	Y23	1.14	1.20	1.26	SATA0 Digital Power
PWRSATA0T	1	U22	1.14	1.20	1.26	SATA0 Tx Driver Power
PWRSATA0A	1	Y21	1.14	1.20	1.26	SATA0 Analog Power
PWRSATA0HA	1	T22	2.38 3.14	2.5 3.3	2.62 3.46	SATA0 High Voltage Analog Power
PWRSATA1	1	W23	1.14	1.20	1.26	SATA1 Digital Power
PWRSATA1T	1	U21	1.14	1.20	1.26	SATA1 Tx Driver Power
PWRSATA1A	1	W21	1.14	1.20	1.26	SATA1 Analog Power
PWRSATA1HA	1	V20	2.38 3.14	2.5 3.3	2.62 3.46	SATA1 High Voltage Analog Power

GNDSATA0	2	U18, T21	-	-	-	SATA0 Ground
GNDSATA1	2	W17, U20	-	-	-	SATA1 Ground
PWRUSB11H33A	1	V19	2.7	3.3	3.6	USB1.1H Power
GNDUSB11H33A	1	AA16				USB1.1H Ground
PWROTG12D	1	M22	1.14	1.20	1.26	USB2.0 OTG Digital Power
PWROTG33A	1	M19	2.7	3.3	3.6	USB2.0 OTG Analog Power
GNDOTG12D	2	T19, R19				USB2.0 OTG Digital Ground
GNDOTG33A	2	T20, R20				USB2.0 OTG Analog Ground
PWRUSB20H12D	1	P21	1.14	1.20	1.26	USB2.0 Host Digital Power
PWRUSB20H33A	1	M20	2.7	3.3	3.6	USB2.0 Host Analog Power
GNDUSB20H12D	1	R21	-	-	-	USB2.0 Host Digital Ground
GNDUSB20H33A	2	T18, R18	-	-	-	USB2.0 Host Analog Ground

Table 3.2 GPIOA(PWRGPA) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
GPIOA[0]	A13	B	IU	GPIOA[0]	SCL(0)					
GPIOA[1]	B11	B	IU	GPIOA[1]	SDA(0)					
GPIOA[2]	B10	B	IU	GPIOA[2]	CLKOUT[0]					
GPIOA[3]	B7	B	IU	GPIOA[3]	CLKOUT[1]					
GPIOA[4]	A11	B	IU	GPIOA[4]	UTM1_VBUS	TCO[0]	PDM[0]			EDIXA[18]
GPIOA[5]	B12	B	IU	GPIOA[5]	REM_IRDI	TCO[1]	PDM[1]			
GPIOA[6]	C12	B	IU	GPIOA[6]		TCO[2]	PDM[2]			EDI_XA[19]
GPIOA[7]	E9	B	IU	GPIOA[7]	SCL(1)	TCO[3]	PDM[3]			
GPIOA[8]	B13	B	IU	GPIOA[8]	SDA(1)					
GPIOA[9]	D10	B	IU	GPIOA[9]	UT_TXD(1)		SD_POW[0]			
GPIOA[10]	D16	B	IU	GPIOA[10]	UT_RXD(1)	CD_BCLI	SD_POW[1]			
GPIOA[11]	D9	B	IU	GPIOA[11]	UT_CTS(1)	CD_LRCKI	SD_POW[2]			
GPIOA[12]	C13	B	IU	GPIOA[12]	UT_RTX(1)	CD_DI	SD_POW[3]			
GPIOA[13]	F22	B	IU	GPIOA[13]	EXTCLKI					
GPIOA[14]	E10	B	IU	GPIOA[14]		TCO[4]	PCIE_WAKE			
GPIOA[15]	F9	B	IU	GPIOA[15]	UTM_VBUS	TCO[5]				

Table 3.3 GPIOB(PWRGPB) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
GPIOB[0]	K4	B	IU	GPIOB[0]	EDI_XD[0]	SD_D(5)[0]	MS_D(5)[0]			
GPIOB[1]	J4	B	IU	GPIOB[1]	EDI_XD[1]	SD_D(5)[1]	MS_D(5)[1]			
GPIOB[2]	B4	B	IU	GPIOB[2]	EDI_XD[2]	SD_D(5)[2]	MS_D(5)[2]			
GPIOB[3]	G4	B	IU	GPIOB[3]	EDI_XD[3]	SD_D(5)[3]	MS_D(5)[3]			
GPIOB[4]	A4	B	IU	GPIOB[4]	EDI_XD[4]	SD_D(5)[4]	MS_D(5)[4]			
GPIOB[5]	K5	B	IU	GPIOB[5]	EDI_XD[5]	SD_D(5)[5]	MS_D(5)[5]			
GPIOB[6]	F4	B	IU	GPIOB[6]	EDI_XD[6]	SD_D(5)[6]	MS_D(5)[6]			
GPIOB[7]	J5	B	IU	GPIOB[7]	EDI_XD[7]	SD_D(5)[7]	MS_D(5)[7]			
GPIOB[8]	J6	B	IU	GPIOB[8]	EDI_XD[8]			SFRM(1)		
GPIOB[9]	K6	B	IU	GPIOB[9]	EDI_XD[9]			SCLK(1)		
GPIOB[10]	G5	B	IU	GPIOB10]	EDI_XD[10]			SDI(1)		
GPIOB[11]	K7	B	IU	GPIOB11]	EDI_XD[11]			SDO(1)		
GPIOB[12]	D7	B	IU	GPIOB[12]	EDI_XD[12]	SD_CMD(5)	MS_BS(5)			
GPIOB[13]	G6	B	IU	GPIOB[13]	EDI_XD[13]	SD_CLK(5)	MS_SCLK(5)			
GPIOB[14]	B5	B	IU	GPIOB[14]	EDI_XD[14]					
GPIOB[15]	C5	B	IU	GPIOB[15]	EDI_XD[15]					
GPIOB[16]	A5	B	IU	GPIOB[16]	EDI_WEN[0]					EDI_RDY[2]
GPIOB[17]	D6	B	IU	GPIOB[17]	EDI_WEN[1]			SFRM(0)		
GPIOB[18]	F6	B	IU	GPIOB[18]	EDI_OEN[0]					EDI_RDY[3]
GPIOB[19]	C6	B	IU	GPIOB[19]	EDI_OEN[1]			SCLK(0)		
GPIOB[20]	A7	B	IU	GPIOB[20]	EDI_XA[0]					
GPIOB[21]	B6	B	IU	GPIOB[21]	EDI_XA[1]	SD_D(6)[4]	MS_D(6)[4]			
GPIOB[22]	C7	B	IU	GPIOB[22]	EDI_XA[2]	SD_D(6)[5]	MS_D(6)[5]			
GPIOB[23]	A10	B	IU	GPIOB[23]	EDI_CSN[0]	SD_D(6)[6]	MS_D(6)[6]			
GPIOB[24]	E7	B	IU	GPIOB[24]	EDI_CSN[1]	SD_D(6)[7]	MS_D(6)[7]			
GPIOB[25]	A8	B	IU	GPIOB[25]	EDI_CSN[2]	SD_D(6)[0]	MS_D(6)[0]			
GPIOB[26]	F7	B	IU	GPIOB[26]	EDI_CSN[3]	SD_D(6)[1]	MS_D(6)[1]			
GPIOB[27]	B8	B	IU	GPIOB[27]	EDI_CSN[4]	SD_D(6)[2]	MS_D(6)[2]			EDIXA[17]
GPIOB[28]	G7	B	IU	GPIOB[28]	EDI_RDY[0]	SD_D(6)[3]	MS_D(6)[3]			
GPIOB[29]	C9	B	IU	GPIOB[29]	EDI_RDY[1]	SD_CMD(6)	MS_BS(6)			
GPIOB[30]	B9	B	IU	GPIOB[30]	EDI_CSN[5]	SD_CLK(6)	MS_SCLK(6)	SDI(0)		EDIXA[16]
GPIOB[31]	C10	B	IU	GPIOB[31]	EDI_CSN[6]			SDO(0)		EDIXA[15]

Table 3.4 GPIOC(PWRGPC) Group I/O Pin Description

NAME	BALL	I/O[11]	INIT[12]	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
GPIOC[0]	Y3	B	IU	GPIOC[0]	LCD0_XD[0]	L0_LPXD[0]			L1_LPXD[0]	HPXD[0]
GPIOC[1]	AA2	B	IU	GPIOC[1]	LCD0_XD[1]	L0_LPXD[1]			L1_LPXD[1]	HPXD[1]
GPIOC[2]	U4	B	IU	GPIOC[2]	LCD0_XD[2]	L0_LPXD[2]			L1_LPXD[2]	HPXD[2]
GPIOC[3]	AC2	B	IU	GPIOC[3]	LCD0_XD[3]	L0_LPXD[3]			L1_LPXD[3]	HPXD[3]
GPIOC[4]	Y2	B	IU	GPIOC[4]	LCD0_XD[4]	L0_LPXD[4]			L1_LPXD[4]	HPXD[4]
GPIOC[5]	R8	B	IU	GPIOC[5]	LCD0_XD[5]	L0_LPXD[5]			L1_LPXD[5]	HPXD[5]
GPIOC[6]	T5	B	IU	GPIOC[6]	LCD0_XD[6]	L0_LPXD[6]			L1_LPXD[6]	HPXD[6]
GPIOC[7]	W3	B	IU	GPIOC[7]	LCD0_XD[7]	L0_LPXD[7]			L1_LPXD[7]	HPXD[7]
GPIOC[8]	U3	B	IU	GPIOC[8]	LCD0_XD[8]	L0_LPXD[8]			L1_LPXD[8]	HPXD[8]
GPIOC[9]	AD2	B	IU	GPIOC[9]	LCD0_XD[9]	L0_LPXD[9]			L1_LPXD[9]	HPXD[9]
GPIOC[10]	AF1	B	IU	GPIOC[10]	LCD0_XD[10]	L0_LPXD[10]			L1_LPXD[10]	HPXD[10]
GPIOC[11]	T4	B	IU	GPIOC[11]	LCD0_XD[11]	L0_LPXD[11]			L1_LPXD[11]	HPXD[11]
GPIOC[12]	AD1	B	IU	GPIOC[12]	LCD0_XD[12]	L0_LPXD[12]			L1_LPXD[12]	HPXD[12]
GPIOC[13]	U2	B	IU	GPIOC[13]	LCD0_XD[13]	L0_LPXD[13]			L1_LPXD[13]	HPXD[13]
GPIOC[14]	V2	B	IU	GPIOC[14]	LCD0_XD[14]	L0_LPXD[14]			L1_LPXD[14]	HPXD[14]
GPIOC[15]	T3	B	IU	GPIOC[15]	LCD0_XD[15]	L0_LPXD[15]			L1_LPXD[15]	HPXD[15]
GPIOC[16]	W2	B	IU	GPIOC[16]	LCD0_XD[16]	L0_LPXD[16]			L1_LPXD[16]	HPXD[16]
GPIOC[17]	AB2	B	IU	GPIOC[17]	LCD0_XD[17]	L0_LPXD[17]			L1_LPXD[17]	HPXD[17]
GPIOC[18]	T2	B	IU	GPIOC[18]	LCD0_XD[18]	L0_LPXD[18]			L1_LPXD[18]	
GPIOC[19]	M1	B	IU	GPIOC[19]	LCD0_XD[19]	L0_LPXD[19]			L1_LPXD[19]	
GPIOC[20]	L1	B	IU	GPIOC[20]	LCD0_XD[20]	L0_LPXD[20]			L1_LPXD[20]	
GPIOC[21]	N2	B	IU	GPIOC[21]	LCD0_XD[21]	L0_LPXD[21]			L1_LPXD[21]	
GPIOC[22]	P7	B	IU	GPIOC[22]	LCD0_XD[22]	L0_LPXD[22]			L1_LPXD[22]	
GPIOC[23]	M2	B	IU	GPIOC[23]	LCD0_XD[23]	L0_LPXD[23]			L1_LPXD[23]	
GPIOC[24]	AC1	B	IU	GPIOC[24]	LCD0_WEN	L0_LACBIAS			L1_LACBIAS	HPWRN
GPIOC[25]	V1	B	IU	GPIOC[25]	LCD0_OEN	L0_LPXCLK			L1_LPXCLK	HPRDN
GPIOC[26]	AA1	B	IU	GPIOC[26]	LCD0_XA	L0_LHSYNC			L1_LHSYNC	HPXA
GPIOC[27]	Y1	B	IU	GPIOC[27]	LCD0_CSN[0]	L0_LVSYNC			L1_LVSYNC	HPCSN0
GPIOC[28]	U1	B	IU	GPIOC[28]	LCD0_CSN[1]	SDO(10)				HPCSN1
GPIOC[29]	H1	B	IU	GPIOC[29]		SDI(10)				
GPIOC[30]	J1	B	IU	GPIOC[30]	EXT_LVS1	SCLK(10)				
GPIOC[31]	N3	B	IU	GPIOC[31]	EXT_LVS0	SFRM(10)				

Table 3.5 GPIOD(PWRGPD/PWRGPDH) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
GPIOD[0]	D13	B	IU	GPIOD[0]	I2S_BCLK(1)					
GPIOD[1]	F20	B	IU	GPIOD[1]	I2S_LRCK(1)					
GPIOD[2]	F23	B	IU	GPIOD[2]	I2S_MCLK(1)					
GPIOD[3]	D22	B	IU	GPIOD[3]	I2S_DAO0(1)					
GPIOD[4]	G10	B	IU	GPIOD[4]	I2S_DAI0(1)					
GPIOD[5]	G19	B	IU	GPIOD[5]	I2S_DAO1(1)	SFRM(11)				
GPIOD[6]	J20	B	IU	GPIOD[6]	I2S_DAI1(1)	SCLK(11)				
GPIOD[7]	D12	B	IU	GPIOD[7]	I2S_DAO2(1)	SDI(11)				
GPIOD[8]	E20	B	IU	GPIOD[8]	I2S_DAI2(1)	SDO(11)				
GPIOD[9]	F10	B	IU	GPIOD[9]	I2S_DAO3(1)	SFRM(6)				
GPIOD[10]	C23	B	IU	GPIOD[10]	I2S_DAI3(1)	SCLK(6)	TS_DATA(2)[7]			
GPIOD[11]	C22	B	IU	GPIOD[11]	SPDIF_TX(1)	SDI(6)	TS_DATA(2)[6]			
GPIOD[12]	C16	B	IU	GPIOD[12]	SPDIF_RX(1)	SDO(6)	TS_SYNC(2)			
GPIOD[13]	G22	B	IU	GPIOD[13]	UT_TXD(4)		TS_DATA(2)[5]	BCLK(0)		
GPIOD[14]	J12	B	IU	GPIOD[14]	UT_RXD(4)		TS_DATA(2)[4]	LRCK(0)		
GPIOD[15]	G24	B	IU	GPIOD[15]	UT_CTS(4)	SFRM(12)	TS_VALID(2)	MCLK(0)		
GPIOD[16]	E22	B	IU	GPIOD[16]	UT_RTS(4)	SCLK(12)	TS_CLK(2)	DAO0(0)		
GPIOD[17]	G23	B	IU	GPIOD[17]	UT_TXD(5)		TS_DATA(2)[3]	DAI0(0)		
GPIOD[18]	F12	B	IU	GPIOD[18]	UT_RXD(5)		TS_DATA(2)[2]	BCLK(2)		
GPIOD[19]	H11	B	IU	GPIOD[19]	UT_CTS(5)	SDI(12)	TS_DATA(2)[1]	LRCK(2)		
GPIOD[20]	J21	B	IU	GPIOD[20]	UT_RTS(5)	SDO(12)	TS_DATA(2)[0]	MCLK(2)		
GPIOD[21]	C24	B	IU	GPIOD[21]			SPDIF_TX(0)	DAO0(2)		
GPIOD[22]	E12	B	IU	GPIOD[22]		SDO(3)	SPDIF_RX(0)	DAI0(2)	SCL(3)	
GPIOD[23]	E16	B	IU	GPIOD[23]	CD_BCLKI	SDI(3)			SDA(3)	
GPIOD[24]	K21	B	IU	GPIOD[24]	CD_LRCKI	SCLK(3)			HDMI_CEC	
GPIOD[25]	D23	B	IU	GPIOD[25]	CD_DI	SFRM(3)			HDMI_HPD	

* GPIOD[21:0] : PWRGPD
* GPIOD[25:22] : PWRGPDH

11 I/O type. B = bi-direction, I = Input, O = Output
12 INIT column represents the corresponding I/O state while the reset signal is asserted.
OL = output low, OH =output high, O=output unknown, IU = input/pull-up, ID = input /pull-down, I = input floating

Table 3.6 GPIOE(PWRGPE) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5
GPIOE[0]	AB25	B	IU	GPIOE[0]	UT_TXD(0)				
GPIOE[1]	W22	B	IU	GPIOE[1]	UT_RXD(0)				
GPIOE[2]	AC25	B	IU	GPIOE[2]	UT_CTX(0)	SFRM(5)			SENSOR_PWDN
GPIOE[3]	AC26	B	IU	GPIOE[3]	UT_RTX(0)	SCLK(5)			FL_TRIG
GPIOE[4]	W11	B	IU	GPIOE[4]	CFIELD				FLASH_TRIG
GPIOE[5]	U23	B	IU	GPIOE[5]					PRELIGHT_TRIG
GPIOE[6]	Y20	B	IU	GPIOE[6]		SDI(5)	SD_CLK(4)	MS_CLK(4)	SHUTTER_TRIG
GPIOE[7]	W24	B	IU	GPIOE[7]		SDO(5)	SD_CMD(4)	MS_BUS(4)	SHUTTER_OPEN
GPIOE[8]	T24	B	IU	GPIOE[8]		SFRM(4)	SD_D(4)[0]	MS_D(4)[0]	CPD[8]
GPIOE[9]	Y25	B	IU	GPIOE[9]		SCLK(4)	SD_D(4)[1]	MS_D(4)[1]	CPD[9]
GPIOE[10]	AG7	B	IU	GPIOE[10]	UT_TXD(3)	SDI(4)	SD_D(4)[2]	MS_D(4)[2]	CPD[10]
GPIOE[11]	AH4	B	IU	GPIOE[11]	UT_RXD(3)	SDO(4)	SD_D(4)[3]	MS_D(4)[3]	CPD[11]
GPIOE[12]	AG5	B	IU	GPIOE[12]	CAM_D[0]		TS_D(1)[0]		
GPIOE[13]	Y22	B	IU	GPIOE[13]	CAM_D[1]		TS_D(1)[1]		
GPIOE[14]	AB24	B	IU	GPIOE[14]	CAM_D[2]		TS_D(1)[2]		
GPIOE[15]	AB26	B	IU	GPIOE[15]	CAM_D[3]		TS_D(1)[3]		
GPIOE[16]	AF7	B	IU	GPIOE[16]	CAM_D[4]		TS_D(1)[4]		
GPIOE[17]	AE7	B	IU	GPIOE[17]	CAM_D[5]		TS_D(1)[5]		
GPIOE[18]	AD7	B	IU	GPIOE[18]	CAM_D[6]		TS_D(1)[6]		
GPIOE[19]	AG6	B	IU	GPIOE[19]	CAM_D[7]		TS_D(1)[7]		
GPIOE[20]	AC7	B	IU	GPIOE[20]	CAM_ICLKI		TSCLK(1)		
GPIOE[21]	AB7	B	IU	GPIOE[21]	CAM_VS		TSSYNC(1)		
GPIOE[22]	Y9	B	IU	GPIOE[22]	CAM_HS		TSVALID(1)		
GPIOE[23]	AH5	B	IU	GPIOE[23]	CAM_ICLKO				

Table 3.7 GPIOF(PWRGPF) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6	FUNC7
GPIOF[0]	M3	B	IU	GPIOF[0]	HDXD[0]	SD_D(3)[0]	HDDXD0	TS_D(0)[0]	MS_D0(3)	EDIXA[3]	ET_TXD[0]
GPIOF[1]	E1	B	IU	GPIOF[1]	HDXD[1]	SD_D(3)[1]	HDDXD1	TS_D(0)[1]	MS_D1(3)	EDIXA[4]	ET_TXD[1]
GPIOF[2]	G2	B	IU	GPIOF[2]	HDXD[2]	SD_D(3)[2]	HDDXD2	TS_D(0)[2]	MS_D2(3)	EDIXA[5]	ET_TXD[2]
GPIOF[3]	N4	B	IU	GPIOF[3]	HDXD[3]	SD_D(3)[3]	HDDXD3	TS_D(0)[3]	MS_D3(3)	EDIXA[6]	ET_TXD[3]
GPIOF[4]	H2	B	IU	GPIOF[4]	HDXD[4]	SD_D(3)[4]	HDDXD4	TS_D(0)[4]	MS_D4(3)	EDIXA[7]	ET_TXEN
GPIOF[5]	L2	B	IU	GPIOF[5]	HDXD[5]	SD_D(3)[5]	HDDXD5	TS_D(0)[5]	MS_D5(3)	EDIXA[8]	ET_TXER
GPIOF[6]	N5	B	IU	GPIOF[6]	HDXD[6]	SD_D(3)[6]	HDDXD6	TS_D(0)[6]	MS_D6(3)	EDIXA[9]	ET_TXCLK
GPIOF[7]	K2	B	IU	GPIOF[7]	HDXD[7]	SD_D(3)[7]	HDDXD7	TS_D(0)[7]	MS_D7(3)	EDIXA[10]	ET_RXCLK
GPIOF[8]	M4	B	IU	GPIOF[8]	HDXD[8]	SD_CMD(3)	HDDXD8	TSVALID(0)	MS_BUS(3)	EDIXA[11]	ETH_RXD[0]
GPIOF[9]	E2	B	IU	GPIOF[9]	HDXD[9]	SD_CLK(3)	HDDXD9	TSCLK(0)	MS_CLK(3)	EDIXA[12]	ETH_RXD[1]
GPIOF[10]	D2	B	IU	GPIOF[10]	HDXD[10]	SDO(7)	HDDXD10	TSSYNC(0)		EDIXA[13]	ETH_RXD[2]
GPIOF[11]	J2	B	IU	GPIOF[11]	HDXD[11]	SDI(7)	HDDXD11			EDIXA[14]	ETH_RXD[3]
GPIOF[12]	C1	B	IU	GPIOF[12]	HDXD[12]	SCLK(7)	HDDXD12		EDIXD16	EDIXA[20]	ET_RXDV
GPIOF[13]	B1	B	IU	GPIOF[13]	HDXD[13]	SFRM(7)	HDDXD13		EDIXD17	EDIXA[21]	ET_RXER
GPIOF[14]	A1	B	IU	GPIOF[14]	HDXD[14]	SDO(8)	HDDXD14		EDIXD18	EDIXA[22]	ET_COL
GPIOF[15]	C2	B	IU	GPIOF[15]	HDXD[15]	SDI(8)	HDDXD15		EDIXD19	EDIXA[23]	ET_CRS
GPIOF[16]	F2	B	IU	GPIOF[16]	HDXD[16]	SCLK(8)	HDDXA0		EDIXD20		ET_REFCLK
GPIOF[17]	M6	B	IU	GPIOF[17]	HDXD[17]	SFRM(8)	HDDXA1		EDIXD21		ET_MDC
GPIOF[18]	A2	B	IU	GPIOF[18]	HPRDN	SD_D(1)[3]	HDDXA2	MS_D(1)[3]	EDIXD22		ET_MDO/I
GPIOF[19]	M5	B	IU	GPIOF[19]	HPWRN	SD_D(1)[2]	HDDCSN1	MS_D(1)[2]	EDIXD23		ET_GTXCLK
GPIOF[20]	K3	B	IU	GPIOF[20]	HPCSN0	SD_D(1)[1]	HDDRDY	MS_D(1)[1]	EDIXD24		ET_TXD[4]
GPIOF[21]	J3	B	IU	GPIOF[21]	HPCSN1	SD_D(1)[0]	HDDCSN0	MS_D(1)[0]	EDIXD25		ET_TXD[5]
GPIOF[22]	G3	B	IU	GPIOF[22]	HPXA	SD_CMD(1)	HDDACK	MS_BUS(1)	EDIXD26		ET_TXD[6]
GPIOF[23]	F3	B	IU	GPIOF[23]	HPINT0	SD_CLK(1)	HDDRQ	MS_CLK(1)	EDIXD27		ET_TXD[7]
GPIOF[24]	B2	B	IU	GPIOF[24]	HPINT1	SDO(9)	HDDIOW		EDIXD28		ETH_RXD[4]
GPIOF[25]	E3	B	IU	GPIOF[25]		SDI(9)	HDDIOR		EDIXD29		ETH_RXD[5]
GPIOF[26]	C3	B	IU	GPIOF[26]		SCLK(9)			EDIXD30	UT_TXD(2)	ETH_RXD[6]
GPIOF[27]	B3	B	IU	GPIOF[27]		SFRM(9)			EDIXD31	UT_RXD(2)	ETH_RXD[7]

* Even if you use the SD port3 as 4bit mode, must set GPIOF[7:0] as FUNC2. In this case, you can't use GPIOF[7:4] as any other function.

Table 3.8 GPIOG(PWRGPG) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
GPIOG[0]	Y8	B	IU	GPIOG[0]	ET_TXD[0]	EDIXD16	SD_D(2)[0]	LCD1_XD[0]	L1_LPXD[0]	MS_D(2)[0]
GPIOG[1]	AH2	B	IU	GPIOG[1]	ET_TXD[1]	EDIXD17	SD_D(2)[1]	LCD1_XD[1]	L1_LPXD[1]	MS_D(2)[1]
GPIOG[2]	AE6	B	IU	GPIOG[2]	ET_TXD[2]	EDIXD18	SD_D(2)[2]	LCD1_XD[2]	L1_LPXD[2]	MS_D(2)[2]
GPIOG[3]	AB6	B	IU	GPIOG[3]	ET_TXD[3]	EDIXD19	SD_D(2)[3]	LCD1_XD[3]	L1_LPXD[3]	MS_D(2)[3]
GPIOG[4]	AG4	B	IU	GPIOG[4]	ET_TXEN	EDIXD20	SD_D(2)[4]	LCD1_XD[4]	L1_LPXD[4]	MS_D(2)[4]
GPIOG[5]	W7	B	IU	GPIOG[5]	ET_TXER	EDIXD21	SD_D(2)[5]	LCD1_XD[5]	L1_LPXD[5]	MS_D(2)[5]
GPIOG[6]	AF6	B	IU	GPIOG[6]	ET_TXCLK	EDIXD22	SD_D(2)[6]	LCD1_XD[6]	L1_LPXD[6]	MS_D(2)[6]
GPIOG[7]	Y7	B	IU	GPIOG[7]	ET_RXCLK	EDIXD23	SD_D(2)[7]	LCD1_XD[7]	L1_LPXD[7]	MS_D(2)[7]
GPIOG[8]	AF5	B	IU	GPIOG[8]	ETH_RXD[0]	EDIXD24	SD_CLK(2)	LCD1_XD[8]	L1_LPXD[8]	MS_CLK(2)
GPIOG[9]	AC6	B	IU	GPIOG[9]	ETH_RXD[1]	EDIXD25	SD_CMD(2)	LCD1_XD[9]	L1_LPXD[9]	MS_BUS(2)
GPIOG[10]	AF3	B	IU	GPIOG[10]	ETH_RXD[2]	EDIXD26	TS_D(3)[0]	LCD1_XD[10]	L1_LPXD[10]	
GPIOG[11]	AC4	B	IU	GPIOG[11]	ETH_RXD[3]	EDIXD27	TS_D(3)[1]	LCD1_XD[11]	L1_LPXD[11]	
GPIOG[12]	Y6	B	IU	GPIOG[12]	ET_RXDV	EDIXD28	TS_D(3)[2]	LCD1_XD[12]	L1_LPXD[12]	
GPIOG[13]	AB5	B	IU	GPIOG[13]	ET_RXER	EDIXD29	TS_D(3)[3]	LCD1_XD[13]	L1_LPXD[13]	
GPIOG[14]	W5	B	IU	GPIOG[14]	ET_COL	EDIXD30	TS_D(3)[4]	LCD1_XD[14]	L1_LPXD[14]	
GPIOG[15]	W6	B	IU	GPIOG[15]	ET_CRS	EDIXD31	TS_D(3)[5]	LCD1_XD[15]	L1_LPXD[15]	
GPIOG[16]	AG3	B	IU	GPIOG[16]	ET_REFCLK	EDI_CSN[7]	TS_D(3)[6]	LCD1_XD[16]	L1_LPXD[16]	
GPIOG[17]	Y5	B	IU	GPIOG[17]	ET_MDC	EDI_CSN[8]	TS_D(3)[7]	LCD1_XD[17]	L1_LPXD[17]	
GPIOG[18]	AB4	B	IU	GPIOG[18]	ET_MDO/I	EDI_CSN[9]	TSVALID(3)	LCD1_XD[18]	L1_LPXD[18]	
GPIOG[19]	AG2	B	IU	GPIOG[19]	ET_GTXCLK	EDI_CSN[10]	TS_CLK(3)	LCD1_XD[19]	L1_LPXD[19]	
GPIOG[20]	W4	B	IU	GPIOG[20]	ET_TXD[4]	EDI_CSN[11]	TSSYNC(3)	LCD1_XD[20]	L1_LPXD[20]	
GPIOG[21]	AF2	B	IU	GPIOG[21]	ET_TXD[5]	TRACECLK	SD_D(0)[7]	LCD1_XD[21]	L1_LPXD[21]	MS_D(0)[7]
GPIOG[22]	T7	B	IU	GPIOG[22]	ET_TXD[6]	TRACECTL	SD_D(0)[6]	LCD1_XD[22]	L1_LPXD[22]	MS_D(0)[6]
GPIOG[23]	AC3	B	IU	GPIOG[23]	ET_TXD[7]	TRACESWO	SD_D(0)[5]	LCD1_XD[23]	L1_LPXD[23]	MS_D(0)[5]
GPIOG[24]	AE2	B	IU	GPIOG[24]	ETH_RXD[4]	TRACEDT[0]	SD_D(0)[4]	LCD1_WEN	L1_LACBIAS	MS_D(0)[4]
GPIOG[25]	AD3	B	IU	GPIOG[25]	ETH_RXD[5]	TRACEDT[1]	SD_D(0)[3]	LCD1_OEN	L1_LPXCLK	MS_D(0)[3]
GPIOG[26]	AH1	B	IU	GPIOG[26]	ETH_RXD[6]	TRACEDT[2]	SD_D(0)[2]	LCD1_XA	L1_LHSYNC	MS_D(0)[2]
GPIOG[27]	Y4	B	IU	GPIOG[27]	ETH_RXD[7]	TRACEDT[3]	SD_D(0)[1]	LCD1_CSN[0]	L1_LVSYNC	MS_D(0)[1]
GPIOG[28]	U6	B	IU	GPIOG[28]		TRACEDT[4]	SD_D(0)[0]	LCD1_CSN[1]	SDO(2)	MS_D(0)[0]
GPIOG[29]	AG1	B	IU	GPIOG[29]		TRACEDT[5]	SD_CLK(0)		SDI(2)	MS_SCLK(0)
GPIOG[30]	U5	B	IU	GPIOG[30]		TRACEDT[6]	SD_CMD(0)	EXTLVS1(1)	SCLK(2)	MS_BS(0)
GPIOG[31]	AB3	B	IU	GPIOG[31		TRACEDT[7]		EXTLVS0(1)	SFRM(2)	

Table 3.9 ADC (PWRADC) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
AIN[0]	K23	B/AI	IU	GPIOE[24]	SCL(2)					
AIN[1]	J25	B/AI	IU	GPIOE[25]	SDA(2)					
AIN[2]	G25	B/AI	IU	GPIOE[26]		SD_CMD(7)	MS_BUS(7)			
AIN[3]	J24	B/AI	IU	GPIOE[27]		SD_CLK(7)	MS_CLK(7)			
AIN[4]	C26	B/AI	IU	GPIOE[28]		SD_D(7)[0]	MS_D(7)[0]			
AIN[5]	K17	B/AI	IU	GPIOE[29]		SD_D(7)[1]	MS_D(7)[1]			
AIN[6]	E26	B/AI	IU	GPIOE[30]		SD_D(7)[2]	MS_D(7)[2]			
AIN[7]	J22	B/AI	IU	GPIOE[31]		SD_D(7)[3]	MS_D(7)[3]			
AIN[8]	F25	AI		AIN[8]						
AIN[9]	F26	AI		AIN[9]						
AIN[10]	J28	AI		AIN[10]						
AIN[11]	K27	AI		AIN[11]						
AIN[12]	L27	AI		AIN[12]						
AIN[13]	J27	AI		AIN[13]						

Table 3.10 ETC (PWRETC) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
BPEN	F1	I	I	Bypass En						
BM[0]	AD26	I	IU	BM[0]						
BM[1]	W25	I	IU	BM[1]						
BM[2]	Y27	I	IU	BM[2]						
BM[3]	AC27	I	IU	BM[3]						
TDO	Y26	O		TDO						
TEST	W26	I	IU	TEST						
RSTN	K25	I	IU	RSTN						
NTRST	U24	I	IU	NTRST						
TMS	U25	I	IU	TMS						
TCK	U27	I	IU	TCK						
TDI	T27	I	IU	TDI						
RTCK	T25	I	IU	BSCAN						

* IU (Input Pull-Up)

Table 3.11 OSC (PWROSC) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
XI	J26	I		XI						
XO	K26	O		XO						

Table 3.12 USB2.0 OTG (PWROTG33A) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
OTG_VBUS	M27			OTG0_VBUS						
OTG_DP	L28			OTG0_DP						
OTG_DM	M28			OTG0_DM						
OTG_ID	K24			OTG0_ATEST						
OTG_REXT	M26			OTG0_TXRTUNE						

Table 3.13 USB2.0 Host (PWRUSB20H33A) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
HST_VBUS	M24			HST_VBUS						
HST_DP	U28			HST_DP						
HST_DM	V28			HST_DM						
HST_REXT	M25			HST_TXRTUNE						

Table 3.14 USB1.1 Host (PWRUSB11H33A) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0	FUNC1	FUNC2	FUNC3	FUNC4	FUNC5	FUNC6
USB11H_DP	AH28			USB11H_DP						
USB11H_DM	AH27			USB11H_DM						

Table 3.15 RTC(PWRRTC) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
RTC_XTI	U26	I		RTC_XTI						
RTC_XTO	R22	O		RTC_XTO						
RTC_PMWKUP	Y24	O	OH	RTC_PMWKUP						
RTC_RSTN	T26	I	IL	RTC_RSTN						

Table 3.16 HDMI OSC (PWRHDMIOSC) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
HDMI_XI	F14			HDMI_XI						
HDMI_XO	E13			HDMI_XO						

Table 3.17 HDMI(PWRHDMI12A) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
HDMI_TXCP	B19			HDMI_TXCP						
HDMI_TXCN	B20			HDMI_TXCN						
HDMI_TX0P	A18			HDMI_TX0P						
HDMI_TX0N	A19			HDMI_TX0N						
HDMI_TX1P	B17			HDMI_TX1P						
HDMI_TX1N	B18			HDMI_TX1N						
HDMI_TX2P	A16			HDMI_TX2P						
HDMI_TX2N	B16			HDMI_TX2N						
HDMI_REXT	F15			HDMI_REXT						

Table 3.18 DAC(PWRADAC) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
DAC_DOUT	AG26			DAC_DOUT						
DAC_COMP	N22			DAC_COMP						
DAC_IREF	N27			DAC_IREF						
DAC_VREF	N26			DAC_VREF						

Table 3.19 MIPI (PWRMIPI) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
MIPIM_D0DP	E17			MIPIM_D0DP						
MIPIM_D0DN	F17			MIPIM_D0DN						
MIPIM_D1DP	C17			MIPIM_D1DP						
MIPIM_D1DN	D17			MIPIM_D1DN						
MIPIM_D2DP	C20			MIPIM_D2DP						
MIPIM_D2DN	D20			MIPIM_D2DN						
MIPIM_D3DP	B21			MIPIM_D3DP						
MIPIM_D3DN	A21			MIPIM_D3DN						
MIPIM_CLKDP	D19			MIPIM_CLKDP						
MIPIM_CLKDN	C19			MIPIM_CLKDN						
MIPI_VREG	E19			MIPI_VREG						
MIPIS_D0DP	B22			MIPIS_D0DP						
MIPIS_D0DN	A22			MIPIS_D0DN						
MIPIS_D1DP	B24			MIPIS_D1DP						
MIPIS_D1DN	B23			MIPIS_D1DN						
MIPIS_D2DP	B26			MIPIS_D2DP						
MIPIS_D2DN	B25			MIPIS_D2DN						
MIPIS_D3DP	A27			MIPIS_D3DP						
MIPIS_D3DN	B27			MIPIS_D3DN						
MIPIS_CLKDP	A25			MIPIS_CLKDP						
MIPIS_CLKDN	A24			MIPIS_CLKDN						

Table 3.20 LVDS (PWRLVDS) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
LVDS_TAP	H27			LVDS_TAP						
LVDS_TAN	H28			LVDS_TAN						
LVDS_TBP	F27			LVDS_TBP						
LVDS_TBN	G27			LVDS_TBN						
LVDS_TCP	E28			LVDS_TCP						
LVDS_TCN	F28			LVDS_TCN						
LVDS_TDP	D27			LVDS_TDP						
LVDS_TDN	E27			LVDS_TDN						
LVDS_TEP	C28			LVDS_TEP						
LVDS_TEN	C27			LVDS_TEN						
LVDS_TCLKP	A28			LVDS_TCLKP						
LVDS_TCLKN	B28			LVDS_TCLKN						
LVDS_ROUT	H18			LVDS_ROUT						

Table 3.21 SATA0 (PWRSATA0) Group I/O Pin Description

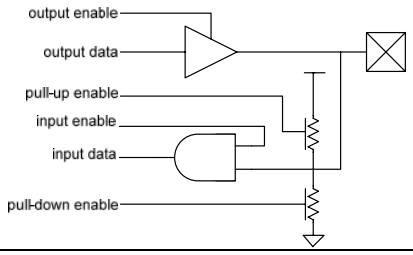
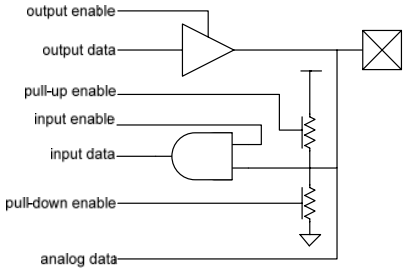
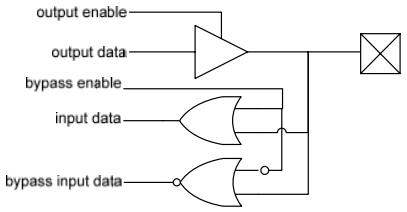
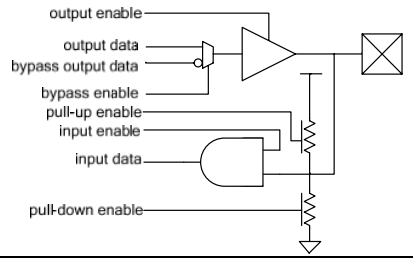
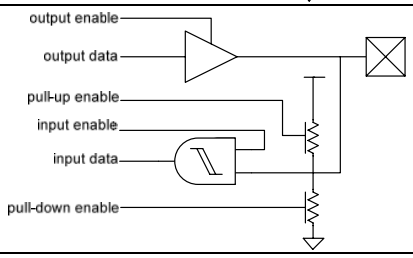
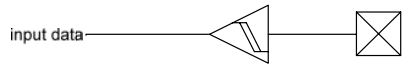
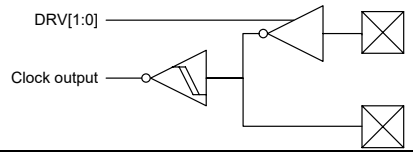
NAME	BALL	I/O	INIT	FUNC0						
SATA0_TXP	Y28									
SATA0_TXN	AA28									
SATA0_RXP	AB27									
SATA0_RXN	AA27									
SATA0_CLKP	W27									
SATA0_CLKN	V27									
SATA0_REFRES	AF28									
SATA0_ATEST	N25									

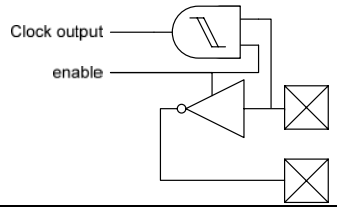
Table 3.22 SATA1 (PWRSATA1) Group I/O Pin Description

NAME	BALL	I/O	INIT	FUNC0						
SATA1_TXP	AC28									
SATA1_TXN	AD28									
SATA1_RXP	AE27									
SATA1_RXN	AD27									
SATA1_CLKP	AG27									
SATA1_CLKN	AG28									
SATA1_REFRES	AF27									
SATA1_ATEST	N24									

3.2 TCC8801 I/O Type

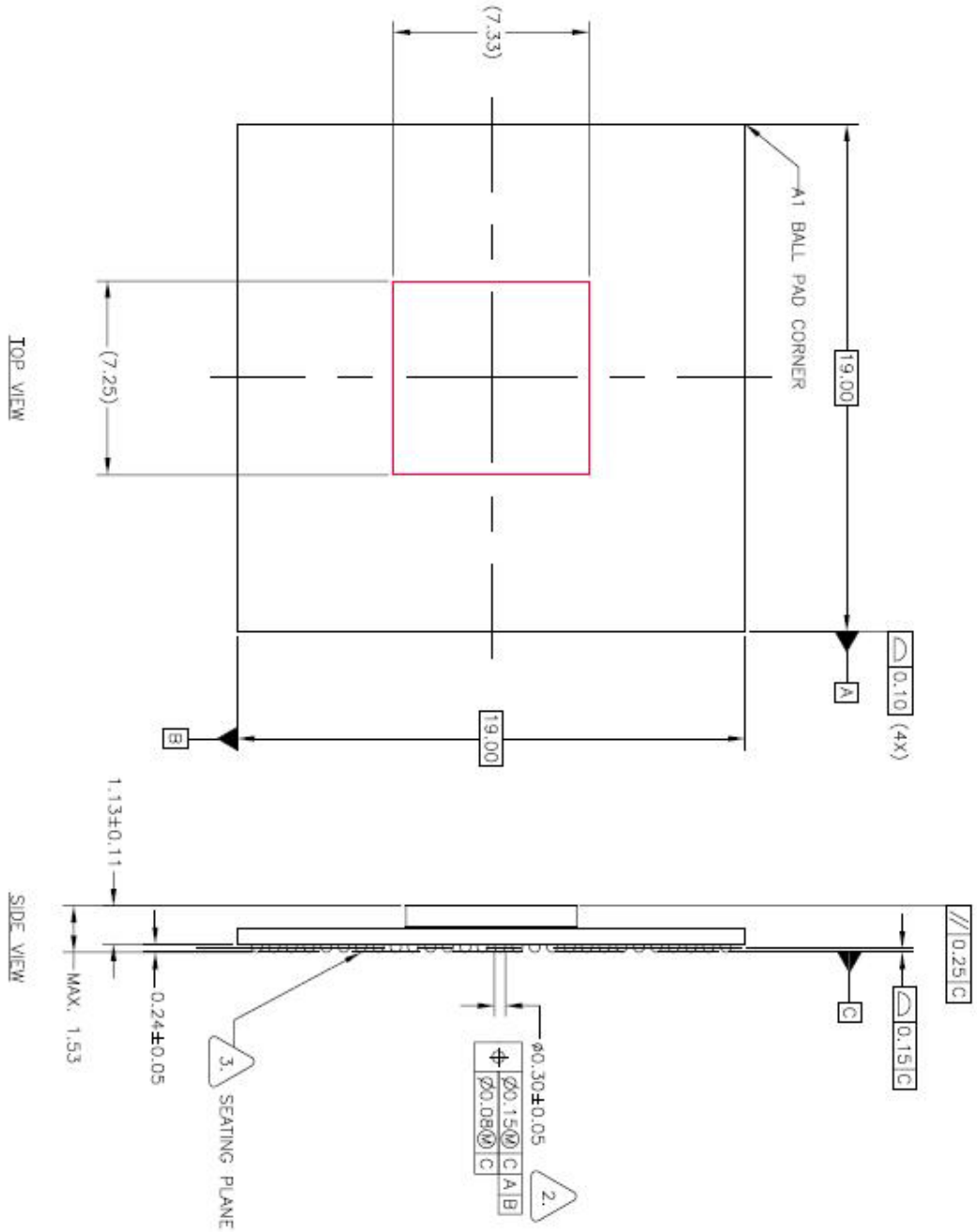
Table 3.23 TCC8801 I/O Type

TYPE	Diagram	DESCRIPTION	PAD Name
A		cmos output with controllable pull-up/down and output PAD	TDO RTCK PMWKUP
B		analog and digital mixed PAD	AIN[0]~AIN[7]
C		cmos input, bypass input and output PAD	GPIOF Group
D		cmos input with controllable pull-up/down, output, and bypass output PAD	GPIOC Group
E		schmitt trigger input with controllable pull-up/down and output PAD	GPIOA Group GPIOB Group GPIOD Group GPIOE Group GPIOG Group
F		schmitt trigger input	BPEN RSTN BM[2]~BM[0] TEST
G		Real Time Clock Oscillator	XTIN,XTOUT

H		oscillator for XIN/XOUT	XIN,XOUT

4 Package Information

4.1 Dimension



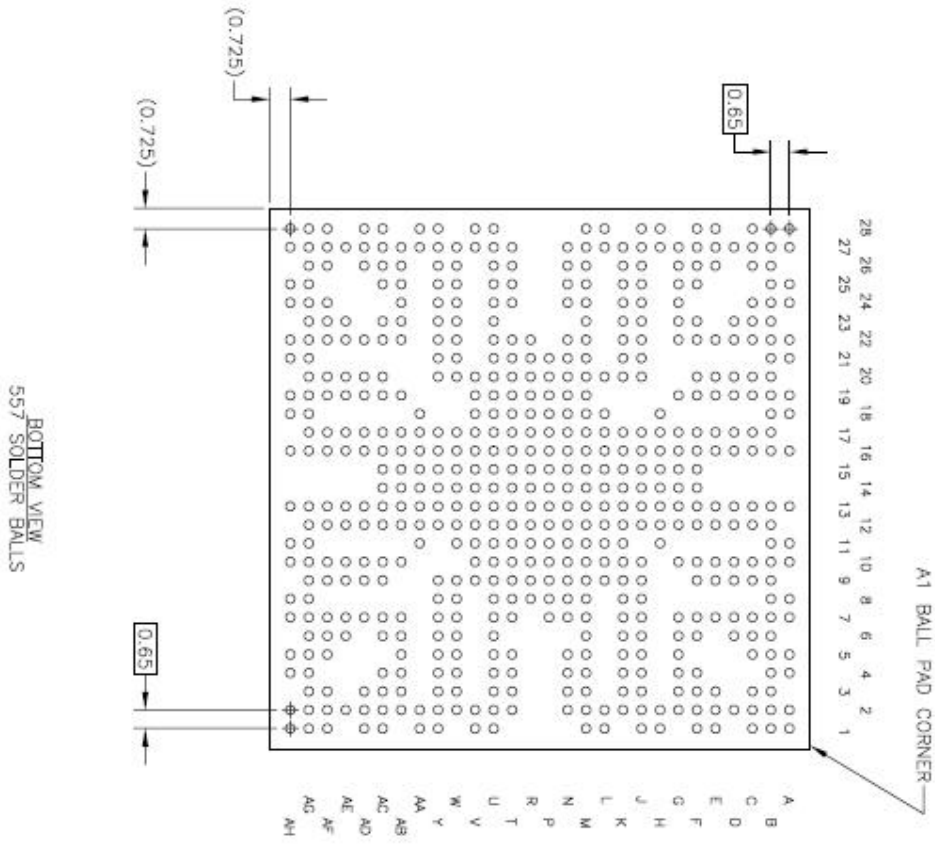


Figure 4.1 TCC8801 Package Dimension

4.2 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28
A	GPIOF[14]	GPIOF[18]		GPIOB[4]	GPIOB[16]		GPIOB[20]	GPIOB[25]		GPIOB[23]	GPIOA[4]		GPIOA[0]			HDMI_TX2P		HDMI_TX0P	HDMI_TX0N		MIPIM_D3DN	MIPIS_D0DN		MIPIS_CLKDN	MIPIS_CLKDP		MIPIS_D3DP	LVDS_TCLKP
B	GPIOF[13]	GPIOF[24]	GPIOF[27]	GPIOB[2]	GPIOB[14]	GPIOB[21]	GPIOA[3]	GPIOB[27]	GPIOB[30]	GPIOA[2]	GPIOA[1]	GPIOA[5]	GPIOA[8]			HDMI_TX2N	HDMI_TX1P	HDMI_TX1N	HDMI_TXCP	HDMI_TXCN	MIPIM_D3DP	MIPIS_D0DP	MIPIS_D1DN	MIPIS_D1DP	MIPIS_D2DN	MIPIS_D2DP	MIPIS_D3DN	LVDS_TCLKN
C	GPIOF[12]	GPIOF[15]	GPIOF[26]		GPIOB[15]	GPIOB[19]	GPIOB[22]		GPIOB[29]	GPIOB[31]		GPIOA[6]	GPIOA[12]			GPIOD[12]	MIPIM_D1DP		MIPIM_CLKDN	MIPIM_D2DP		GPIOD[11]	GPIOD[10]	GPIOD[21]		AIN[4]	LVDS_TEN	LVDS_TEP
D		GPIOF[10]				GPIOB[17]	GPIOB[12]		GPIOA[11]	GPIOA[9]		GPIOD[7]	GPIOD[0]			GPIOA[10]	MIPIM_D1DN		MIPIM_CLKDP	MIPIM_D2DN		GPIOD[3]	GPIOD[25]				LVDS_TDP	
E	GPIOF[1]	GPIOF[9]	GPIOF[25]				GPIOB[24]		GPIOA[7]	GPIOA[14]		GPIOD[22]	HDMI_XO			GPIOD[23]	MIPIM_D0DP		MIPI_VREG	GPIOD[8]		GPIOD[16]				AIN[6]	LVDS_TDN	LVDS_TCP
F	BPEN	GPIOF[16]	GPIOF[23]	GPIOB[6]		GPIOB[18]	GPIOB[26]		GPIOA[15]	GPIOD[9]		GPIOD[18]	HDMI_XI		HDMI_REXT	MIPIM_D0DN	PWRLVDS12A		PWRLVDS33A	GPIOD[1]		GPIOA[13]	GPIOD[2]			AIN[9]	LVDS_TBP	LVDS_TCN
G		GPIOF[2]	GPIOF[22]	GPIOB[3]	GPIOB[10]	GPIOB[13]	GPIOB[28]			GPIOD[4]		PWRHDMIPLL	GNDHDMI12A		GNDMIPI	GNDMIPI	PWRLVDS12A		GPIOD[5]			GPIOD[13]	GPIOD[17]	GPIOD[15]	AIN[2]	ADC_VREF	LVDS_TBN	
H	GPIOC[29]	GPIOF[4]			GPIOB[7]	GPIOB[8]	GNDGPB	GNDGPA	PWRGPD	PWRGPDH	GPIOD[19]	PWRHDMIOSC	GNDHDMI12A		GNDMIPI	PWRADC	PWRMIPI12D	LVDS_ROUT										LVDS_TAP	LVDS_TAN
J	GPIOC[30]	GPIOF[11]	GPIOF[21]	GPIOB[1]	GPIOB[7]	GPIOB[8]	GNDGPB	GNDGPA	PWRGPD	PWRGPDH	GPIOD[14]	GPIOD[20]	GNDCOREAB		GNDCOREAB	PWRMIPI18D	PWRMIPI12D	GPIOD[6]	GPIOD[7]	AIN[7]	GPIOD[20]	PWROSC	AIN[3]	AIN[1]	XI	AIN[13]	AIN[10]	

	OTG_DP	OTG_DM					USB20H_DP	USB20H_DM						K
AIN[11]	AIN[12]	OTG_VBUS	DAC_IREF				TDI	TCK	SATA0_CLKN	SATA0_CLKP				L
XO		OTG_REXT	DAC_VREF				RTC_RSTN	RTC_XTI		TEST				M
RSTN		USB20H_REXT	SATA0_ATEST				RTCK	TMS		BM[1]				N
OTG_ID		USB20H_VBUS	SATA1_ATEST				GPIOE[8]	NTRST		GPIOE[7]				P
AIN[0]		PWRRTC					GPIOE[5]			PWRSATA1				R
PWRETC		PWROTG12D	DAC_COMP				PWRSATA0HA	PWRSATA0T		GPIOE[1]				T
GPIOD[24]		PWRPLL0	GNDOSC	PWRUSB20H12D			GNDSATA0	PWRSATA1T		PWRSATA1A				U
GNDLVDS33A	PWRPLL1	PWRUSB20H33A	GNDLVDS12A	GNDPLL	GNDOTG33A		GNDOTG33A	GNDSATA1	PWRSATA1HA	PWRDDAC				V
		PWROTG33A	GNDADC	GNDPLL	GNDOTG12D		GNDOTG12D	GNDDDAC	PWRUSB11H33A					W
AIN[5]	PWRCOREA	PWRCOREA	GNDCOREAB	PWRCOREA	PWRCOREA		PWRCOREA	PWRCOREA	GNDCOREAB	GNDSATA1				
PWRMIPI12D	PWRCOREA	PWRCOREA	GNDCOREAB	GNDCOREAB	PWRCOREA		PWRCOREA	PWRCOREA	GNDCOREAB	GNDCOREAB				
PWRMIPI12D	GNDCOREAB	PWRCOREA	PWRCOREA	PWRCOREA	PWRCOREA		PWRCOREA	GNDCOREAB	GNDCOREAB	PWRMEMQ				
PWRMIPI12D	GNDCOREAB	PWRCOREA	GNDCOREAB	GNDCOREAB	PWRCOREA		PWRCOREA	PWRCOREA	GNDCOREAB	PWRMEMQ				
GNDCOREAB	PWRCOREA	PWRCOREA	GNDCOREAB	PWRCOREB	PWRCOREB		PWRCOREB	PWRCOREB	PWRCOREB	PWRCOREA				
GNDCOREAB	GNDCOREAB	PWRCOREA	PWRCOREA	PWRCOREA	PWRCOREA		PWRCOREB	PWRCOREB	PWRCOREB	PWRCOREA				
GNDCOREAB	GNDCOREAB	PWRCOREA	PWRCOREA	PWRCOREA	GNDCOREAB		GNDCOREAB	GNDCOREAB	PWRCOREB	GPIOE[4]				
GNDGPDH	GNDHDMIOSC	PWRCOREA	PWRCOREA	PWRCOREA	GNDCOREAB		GNDCOREAB	GNDCOREAB	GNDCOREAB					
GNDGPD	PWRGPA	PWRGPB	PWRCOREA	GNDGPE	GNDGPG	GNDMEMZQ	PWRGPC	PWRGPC	PWRGPC	PWRMEMZQ				
GNDGPB		PWRGPB	GNDGPF	GNDGPC	GPIOC[5]	GNDGPG	PWRGPG	PWRGPG		PWRGPE				
GPIOB[11]		PWRGPF	GNDGPC	GPIOC[22]		GPIOG[22]	PWRGPG	PWRGPG		GPIOG[5]				
GPIOB[9]		GPIOF[17]					GPIOG[28]	GPIOG[28]		GPIOG[15]				
GPIOB[5]		GPIOF[19]	GPIOF[6]			GPIOC[6]	GPIOG[30]	GPIOG[30]		GPIOG[14]				
GPIOB[0]		GPIOF[8]	GPIOF[3]			GPIOC[11]	GPIOC[2]	GPIOC[2]		GPIOG[20]				
GPIOF[20]		GPIOF[0]	GPIOC[31]			GPIOC[15]	GPIOC[8]	GPIOC[8]		GPIOC[7]				
GPIOF[7]	GPIOF[5]	GPIOC[23]	GPIOC[21]			GPIOC[18]	GPIOC[13]	GPIOC[13]	GPIOC[14]	GPIOC[16]				
	GPIOC[20]	GPIOC[19]					GPIOC[28]	GPIOC[28]	GPIOC[25]					

SATA0_TXP	SATA0_TXM		SATA1_TXP	SATA1_TXM			SATA0_REFRES	SATA1_CLKN	USB11H_DP	Y
BM[2]	SATA0_RXM	SATA0_RXP	BM[3]	SATA1_RXM	SATA1_RXP	SATA1_REFRES	SATA1_CLKP	USB11H_DM	AA
TDO		GPIOE[15]	GPIOE[3]	BM[0]		TRACECLKIN	DAC_OUT		AB
GPIOE[9]		GPIOE[0]	GPIOE[2]				DRAM_GATEO	DRAM_DQSB[1]	AC
RTC_PWWKUP		GPIOE[14]				DRAM_XD[3]	DRAM_XD[5]	DRAM_DQS[1]	AD
PWRSATA0		DRAM_XD[7]	DRAM_XD[1]		DRAM_DQM[0]	DRAM_XD[2]	DRAM_XD[0]		AE
GPIOE[13]		DRAM_XD[8]	DRAM_XD[10]	DRAM_XD[14]	DRAM_XD[12]	DRAM_XD[4]	DRAM_XD[6]	DRAM_DQSB[0]	AF
PWRSATA0A							DRAM_XD[15]	DRAM_DQS[0]	AG
GPIOE[6]			DRAM_GATEI	DRAM_DQM[1]	DRAM_XD[11]	DRAM_XD[9]	DRAM_XD[13]		AH
		DRAM_XA[11]	DRAM_XA[6]	DRAM_XA[1]	DRAM_XA[4]	DRAM_XA[12]	DRAM_ODT[1]	DRAM_CLKB	
	DRAM_XA[8]						DRAM_ODT[0]	DRAM_CLK	
GNDADAC	GNDETC	DRAM_BA[1]	DRAM_CKE	DRAM_XA[10]	DRAM_XA[14]	DRAM_WEN	DRAM_XA[2]		
PWRMEMQ	GNDUSB11H33A	GNDCOREAB	DRAM_XA[3]	DRAM_XA[13]	DRAM_CSN[0]	DRAM_XA[7]	DRAM_XA[0]	DRAM_XA[5]	
PWRMEMQ	GNDCOREAB	GNDCOREAB	DRAM_BA[2]						
PWRMEMQ	PWRMEMQ	PWRMEMQ	DRAM_BA[0]						
PWRCOREA	PWRMEMQ	PWRMEMQ	GNDMEMCKE	DRAM_RASN	DRAM_CASN	DRAM_CSN[1]	DRAM_VREF1	DRAM_VREF0	
PWRMEMCKE	DRAM_XD[20]	DRAM_XD[21]	DRAM_XD[23]	DRAM_XD[19]	DRAM_XD[17]	DRAM_DQM[2]	DRAM_XA[9]		
	DRAM_XD[22]						DRAM_DQS[3]	DRAM_DQSB[3]	
		GNDCOREAB	DRAM_XD[18]	DRAM_XD[16]	DRAM_XD[26]	DRAM_XD[28]	DRAM_DQS[2]	DRAM_DQSB[2]	
GPIOE[22]			DRAM_XD[24]	DRAM_XD[30]	DRAM_DQM[3]	DRAM_XD[25]	DRAM_XD[27]		
GPIOG[0]							DRAM_XD[31]	DRAM_XD[29]	
GPIOG[7]		GPIOE[21]	GPIOE[20]	GPIOE[18]	GPIOE[17]	GPIOE[16]	GPIOE[10]	DRAM_ZQ	
GPIOG[12]		GPIOG[3]	GPIOG[9]		GPIOG[2]	GPIOG[6]	GPIOE[19]		
GPIOG[17]		GPIOG[13]				GPIOG[8]	GPIOE[12]	GPIOE[23]	
GPIOG[27]		GPIOG[18]	GPIOG[11]				GPIOG[4]	GPIOE[11]	
GPIOC[0]		GPIOG[31]	GPIOG[23]	GPIOG[25]		GPIOG[10]	GPIOG[16]		
GPIOC[4]	GPIOC[1]	GPIOC[17]	GPIOC[3]	GPIOC[9]	GPIOG[24]	GPIOG[21]	GPIOG[19]	GPIOG[1]	
GPIOC[27]	GPIOC[26]		GPIOC[24]	GPIOC[12]		GPIOC[10]	GPIOG[29]	GPIOG[26]	

Figure 4.2 TCC8801 Ball Map

5 Electrical Specification

5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
DC Supply Voltage for I/O (Various I/O power excepts for analog – ADC, DAC, PLL, USB)	V_{DDIO}	4.6	V
DC Supply Voltage for Internal Digital Logic (VDD_CORE)	V_{DDI}	1.8	V
DC Supply Voltage for Analog Part of ADC (VDD_ADC)	V_{DDADC}	4.6	V
DC Supply Voltage for PLL (VDD_PLL)	V_{DDPLL}	1.8	V
DC Supply Voltage for USB2.0 (VDD33_USB0/1)	V_{DDUSB}	4.6	V
DC Supply Voltage for RTC (VDD_RTC)	V_{DDRTC}	4.6	V
Digital Input Voltage for Input Buffer	V_{IN}	4.6	V
Digital Input Voltage for OTG_VBUS	V_{OTG_VBUS}	6.0	V
Digital Output Voltage for Output Buffer	V_{OUT}	4.6	V
In/Out Current for Digital I/O	$I_{I/O}$	±20	mA
Analog Input Voltage for ADC	V_{IN_ADC}	0 ~ V_{DDADC}	V
Storage Temperature	T_{STG}	-55 to 150	°C

Note:
Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Each condition value is applied with the other values kept within the following operating conditions and functional operation under any of these conditions is not implied.

(1) All voltages are measured with respect to VSS unless otherwise specified.
(2) V_{DDI} must always be less than V_{DDIO}
(3) The voltage difference between analog and digital grounds must always be within 0.3V.

5.2 Recommended Operating Conditions

Table 5.1 Recommended Operating Conditions[13]

Parameter	Symbol	MIN	TYP	MAX	Unit
Output Load Resistance for DAC [±1% tolerance]	R_{LOAD}	-	37.5	-	Ω
Core (PWRCOREA/B) and PLL (PWRPLL0/1) and USB(PWRUSB20H12D/PWROTG12D) supply Voltage	V_{DDI} V_{DDPLL} $V_{DDUSB12}$	TBD	1.0	TBD	V
		1.05	1.1	1.15	
		1.14	1.2	1.26	
		1.23	1.3	1.37	
		1.33	1.4	1.47	
		1.43	1.5	1.57	
Operating Ambient Temperature [Extended]	T_A	-30		85	°C
Operating Ambient Temperature [Industrial]	T_A	-40	-	85	°C

13 The recommended operating conditions for power/ground are described on the Power/Ground Information in the Pin Descriptions.

5.3 Recommended Operating Frequency

Table 5.2 Recommended Operating Frequency

Parameter	Condition	Symbol	MIN	TYP	MAX	Unit
XIN Oscillator	@ 1.0V(TYP)	F_{XIN}	12	12	12	MHz
	@ 1.1V(TYP)					
	@ 1.2V(TYP)					
	@ 1.3V(TYP)					
	@ 1.4V(TYP)					
	@ 1.5V(TYP)					
XTIN Oscillator	@ 1.2V(TYP)	F_{XTIN}	32.768		32.768*128	KHz
PLL0/4/5 VCO Range	@ 1.0V(TYP)	$F_{PLL045VCO}$	TBD		TBD	MHz
	@ 1.1V(TYP)		TBD		TBD	
	@ 1.2V(TYP)		**1000**		**2000**	
	@ 1.3V(TYP)		TBD		TBD	
	@ 1.4V(TYP)		TBD		TBD	
	@ 1.5V(TYP)		TBD		TBD	
PLL1/2/3 VCO Range	@ 1.0V(TYP)	$F_{PLL123VCO}$	TBD		TBD	MHz
	@ 1.1V(TYP)		TBD		TBD	
	@ 1.2V(TYP)		**330**		**660**	
	@ 1.3V(TYP)		TBD		TBD	
	@ 1.4V(TYP)		TBD		TBD	
	@ 1.5V(TYP)		TBD		TBD	
Input Clock of Bus Clock Generator (1 ~ 10)[14] (PWRCOREA)	@ 1.0V(TYP)	$F_{BCLKGEN}$			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**1600**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Input Clock of CPU Clock Generator[15] (PWRCOREA)	@ 1.0V(TYP)	F_{CPUGEN}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**1600**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Input Clock of PLL Divider (PWRCOREA)	@ 1.0V(TYP)	$F_{PLLDIVIN}$			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**1400**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Input Clock of I/O Clock Generator[16] (PWRCOREA)	@ 1.0V(TYP)	$F_{IOCLKGEN}$			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**500**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Cortex-A8 Core Clock (PWRCOREA)	@ 1.0V(TYP)	F_{CPU}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**800**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Bus Clock of DDI Bus (PWRCOREA)	@ 1.0V(TYP)	F_{BUS_DDI}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**290**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Bus Clock of Graphic Bus **(PWRCOREB)**	@ 1.0V(TYP)	F_{BUS_GRP}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**320**	

14 The related clocks are F_{BUS_DDI}, F_{BUS_GRP}, F_{BUS_MEM}, F_{BUS_VBUS}, F_{BUS_VCODEC},F_{BUS_SMU}, F_{BUS_IOB}.
15 The related clock is F_{CPU}.
16 The prefix of related clocks is $F_{IO\_}$.

	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Bus Clock of I/O Bus (PWRCOREA)	@ 1.0V(TYP)	F_{BUS_IOB}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**190**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Bus Clock of High Speed I/O Bus (PWRCOREA)	@ 1.0V(TYP)	F_{BUS_HSIOB}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**240**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Bus Clock of SMU Controller (PWRCOREA)	@ 1.0V(TYP)	F_{BUS_SMU}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**200**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Bus Clock of Video Bus **(PWRCOREB)**	@ 1.0V(TYP)	F_{BUS_VBUS}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**300**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Bus Clock of Camera Bus (PWRCOREA)	@ 1.0V(TYP)	F_{BUS_CAMBUS}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**330**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Core Clock of Video Codec **(PWRCOREB)**	@ 1.0V(TYP)	F_{BUS_VCODEC}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**290**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Bus Clock of Memory Interface (LPDDR2/DDR2/DDR3) (PWRCOREA)	@ 1.0V(TYP)	F_{BUS_MEM}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**320**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Bus Clock of Memory Interface (LPDDR) (PWRCOREA)	@ 1.0V(TYP)	F_{BUS_MEM}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**200**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of Camera Interface 0[17] (PWRCOREA)	@ 1.0V(TYP)	F_{IO_CIF}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**150**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of EHI[17] (PWRCOREA)	@ 1.0V(TYP)	F_{IO_EHI}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**200**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of GPSB Controller[17] (PWRCOREA)	@ 1.0V(TYP)	F_{IO_GPSB}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**160**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	

17 The operating frequencies of external interface are not same as this. More detailed information is described on the timing characteristics of I/O interface. Refer to the corresponding timing information.

Operating Clock of Memory Stick Controller[17] (PWRCOREA)	@ 1.0V(TYP)	F_{IO_MSTICK}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**100**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of SD/MMC Controller[17] (PWRCOREA)	@ 1.0V(TYP)	F_{IO_SDMMC}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**180**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of UART Controller[17] (PWRCOREA)	@ 1.0V(TYP)	F_{IO_UART}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**200**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of LCD Controller[17] (PWRCOREA)	@ 1.0V(TYP)	F_{IO_LCD}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**160**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of PMU (PWRCOREA)	@ 1.0V(TYP)	F_{IO_PMU}	12	12	12	MHz
	@ 1.1V(TYP)					
	@ 1.2V(TYP)					
	@ 1.3V(TYP)					
	@ 1.4V(TYP)					
	@ 1.5V(TYP)					
Operating Clock of Timer (PWRCOREA)	@ 1.0V(TYP)	F_{IO_TIMER}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**160**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of TSIF(Not GPSB) (PWRCOREA)	@ 1.0V(TYP)	F_{IO_TSIF}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**100**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of SPDIF Transmitter/Receiver[17] (PWRCOREA)	@ 1.0V(TYP)	F_{IO_SPDIF}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**100**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of Audio (ADMA/DAI/CDIF) [17] (PWRCOREA)	@ 1.0V(TYP)	F_{IO_AUDIO}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**75**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	
Operating Clock of I2C[17] (PWRCOREA)	@ 1.0V(TYP)	F_{IO_I2C}			TBD	MHz
	@ 1.1V(TYP)				TBD	
	@ 1.2V(TYP)				**200**	
	@ 1.3V(TYP)				TBD	
	@ 1.4V(TYP)				TBD	
	@ 1.5V(TYP)				TBD	

➔The maximum operating frequency can be changed without any notice until approved for mass production.

5.4 Electrical Characteristics for Power Supply

Table 5.3 Peak Power Consumption

Parameter	Power	Condition	MIN	TYP	MAX	Unit
Internal Core Power	PWRCOREA/B	@ 1.2V			TBD	mA
GPIO Power	PWRGPn, (n=A,B,C,D,E,F,G,ETC,DH)	@ 1.8V @ 2.7V @ 3.3V			TBD	mA
Memory I/O Power	PWRMEMQ, PWRMEMZQ PWRMEMCKE	@ 1.2V @ 1.5V @ 1.8V			TBD	mA
Oscillator Power (XI/XO)	PWROSC	@ 1.8V			TBD	mA
USB 1.2 Power of nanoPHY	PWROTG12D PWRUSB20H12D	@ 1.2V			TBD	mA
USB 3.3 Power of nanoPHY	PWROTG33A PWRUSB20H33A	@ 3.3V			TBD	mA
RTC Power	PWRRTC	@ 2.7V			TBD	mA

➔The rests of the power which are not described in the above table are shown in the corresponding sub-section.

➔***The value in the above table does not mean the average power***. Refer to this at the designing of the power circuit.

5.5 Electrical Characteristics for General I/O

Table 5.4 DC Electrical Specification for General I/O

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}		$0.7V_{DDIO}$		V_{DDIO}+0.3	V
Low Level Input Voltage	V_{IL}		-0.3		$0.3V_{DDIO}$	V
Hysteresis Voltage	△V		$0.1V_{DDIO}$			V
High Level Input Current	I_{IH}	VIN =VDDIO, pull-down disabled	-10		10	μA
		VIN = VDDIO, pull-down enabled	TBD		TBD	μA
Low Level Input Current	I_{IL}	VIN = VSSIO, pull-up disabled	-10		10	μA
		VIN = VSSIO, pull-up enabled	TBD		TBD	μA
High Level Output Voltage	V_{OH}	IOH = -100uA	V_{DDIO}–0.2			V
Low Level Output Voltage	V_{OL}	IOL = 100uA			0.2	V
Tri-state Output Leakage Current	I_{OZ}	VOUT = VSSIO or VDDIO	-10		10	μA
Input capacitance	C_{IN}	Any input and Bidirectional buffers			5	pF
Output capacitance	C_{OUT}	Any output buffer			5	pF
XI/XO Frequency	F_{OSC1}		-	12	-	MHz
XTIN/XTOUT Frequency	F_{OSC2}	Normal High Drive = Normal * 128	-	32.768 4194.304	-	kHz

Ta = 25oC, VSS = 0.0V unless otherwise specified.

Note:

(1) 12MHz is recommended for XI/XO frequency.
(2) PLL Output Frequencies are determined by XI/XO frequency.

5.6 Electrical Characteristics for PLL

Table 5.5 DC Electrical Characteristics for PLL0/4/5

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Power Down Current	I_{PD}	V_{DDPLL} = 1.2V			120	μA
Power Consumption	P_{DD}	V_{DDPLL} = 1.2V			2.4	mW

Ta = 25oC unless otherwise specified.

Table 5.6 AC Electrical Characteristics for PLL0/4/5

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Input Frequency	Fin	V_{DDPLL} = 1.2V		12		MHz
VCO output frequency	Fvco	V_{DDPLL} = 1.2V	1000	-	2000	MHz
Output Frequency	Fout	V_{DDPLL} = 1.2V	32		2000	MHz
Locking Time	T_{LT}	V_{DDPLL} = 1.2V			400	Cycle

Ta = 25oC unless otherwise specified.

Table 5.7 DC Electrical Characteristics for PLL1/2/3

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Power Down Current	I_{PD}	V_{DDPLL} = 1.2V			120	μA
Power Consumption	P_{DD}	V_{DDPLL} = 1.2V			1.2	mW

Ta = 25oC unless otherwise specified.

Table 5.8 AC Electrical Characteristics for PLL1/2/3

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Input Frequency	Fin	V_{DDPLL} = 1.2V		12		MHz
VCO output frequency	Fvco	V_{DDPLL} = 1.2V	330	-	660	MHz
Output Frequency	Fout	V_{DDPLL} = 1.2V	12		660	MHz
Locking Time	T_{LT}	V_{DDPLL} = 1.2V			400	cycle

Ta = 25oC unless otherwise specified.

5.7 Electrical Characteristics for Video DAC

Table 5.9 DC Electrical Characteristics for DAC

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Resolution	Bit		-	-	10	bits
Conversion Rate	F_{CLK}		-	-	27	MHz
Differential Non-Linearity	DNL		-	-	±1	LSB
Integral Non-Linearity	INL		-	-	±2	LSB
Full Scale Output Voltage	V_O		1.17	1.3	1.43	V
Output Load	R_{LOAD}	±1% tolerance		37.5		Ω
External Reference Voltage	V_{REF}		-	1.26	-	V

(VDDDAC =3.0V, VSSDAC =0V, Power Down = OFF, Top=30° C,
R(IREF) =1.2kΩ, Load Resistance=37.5Ω unless otherwise specified.)

5.8 Electrical Characteristics for ADC(for Touch Screen)

Table 5.10 DC Electrical Characteristics for ADC

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Resolution	Bit		-	-	12	bits
Differential Non-Linearity	DNL	VREF=3.3V, GND=0V	-	-	±0.5	LSB
Integral Non-Linearity	INL	VREF=3.3V, GND=0V	-	-	±2	LSB
Offset Voltage	TOPOFF BOTOFF	VREF=3.3V, GND=0V	-	-	20	LSB

(Converter Specifications: VDDADC= 3.3V, VSSADC= 0V, Top=25°C, VREF=3.3V, GND=0.0V unless otherwise specified)

Table 5.11 AC Electrical Characteristics for ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum conversion rate	fc	f_{CKIN} = 5MHz	–	–	1	MSPS
Standby supply current	–	STBY = VDD	–	-	10	uA
Dynamic supply current	IVDD	f_{CKIN} = 5MHz (without system load)	–	4	6	mA
Total harmonic distortion	THD	f_{CKIN} = 5MHz f_{AIN} = 100kHz	–	TBD	TBD	dB
Signal-to-noise & distortion ratio	SNDR	f_{CKIN} = 5MHz f_{AIN} = 100kHz	54	60	–	dB

(Converter Specifications: VDDADC =3.3V, VSSADC=0V, Top=25°C, VREF=3.3V, GND=0.0V unless otherwise specified) VDDIO = 3.3V±0.3V

5.9 Electrical Characteristics for HDMI PHY

Table 5.12 DC Electrical Characteristics for HDMI PHY

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Normal Mode Operating Power	P_{CC}	Internal Video PLL ON Internal Video PLL OFF	-	TBD TBD	-	mW
Power-Down Mode Power	P_{PD}	-	-	TBD	-	mW

Table 5.13 AC Electrical Characteristics for HDMI Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HDMI Oscillator Frequency	F_R	-	–	27		MHz
Frequency Tolerance	F_{TOL}		-100		100	ppm
Duty Cycle	D_C		40		60	%
Jitter	J_{CLKI}	Peak-to-Peak Jitter RMS Jitter			50 3.5	ps ps

5.10 Electrical Characteristics for SATA

Table 5.14 DC Electrical Characteristics for SATA

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
TX serial data output voltage	DV_{TX}	1.5Gbps 3.0Gbps	TBD TBD		TBD TBD	mVp-p
RX serial data input voltage	DV_{RX}	1.5Gbps 3.0Gbps	TBD TBD		TBD TBD 0	mVp-p
Dynamic Current	I_{DD}	Normal Mode Partial Mode		TBD TBD		mW
Power Down Current	I_{PD}	Slumber Mode		TBD		mW

All values in the above table are measured at typical condition.

Table 5.15 AC Electrical Characteristics for SATA Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	F_R		–	25 100		MHz
Frequency Tolerance	F_{TOL}		TBD		TBD	ppm
Duty Cycle	D_C		TBD		TBD	%
Clock Transition Time	T_{CLKT}	Rising Falling			TBD TBD	ns
Jitter	J_{CLKI}	Peak-to-Peak Jitter RMS Jitter			TBD TBD	ps ps

Table 5.16 AC Electrical Characteristics for SATA TX/RX

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Unit Interval	UI	1.5Gbps 3.0Gbps	–	TBD TBD		ps
TX Serial Output Rise Time (20% → 80%)	$T_{TX.RISE}$	1.5Gbps 3.0Gbps	TBD		TBD TBD	ps
TX Serial Output Fall Time (80% → 20%)	D_C	1.5Gbps 3.0Gbps	TBD TBD		TBD TBD	ps
TX Serial Data Output Voltage (Differential Peak-to-Peak)	D_{VTX}	1.5Gbps 3.0Gbps	TBD TBD		TBD TBD	mVp-p
RX Serial Data Input Voltage (Differential Peak-to-Peak)	T_{RJ}	1.5Gbps 3.0Gbps	TBD TBD		TBD TBD	mVp-p

5.11 Electrical Characteristics for LCD Interface

The following figure shows the timing diagram for TFT-LCD with RGB interface. All the timing parameters can be configured by LHTIME1, LHTIME2, LVTIME1 ~ 4 registers.

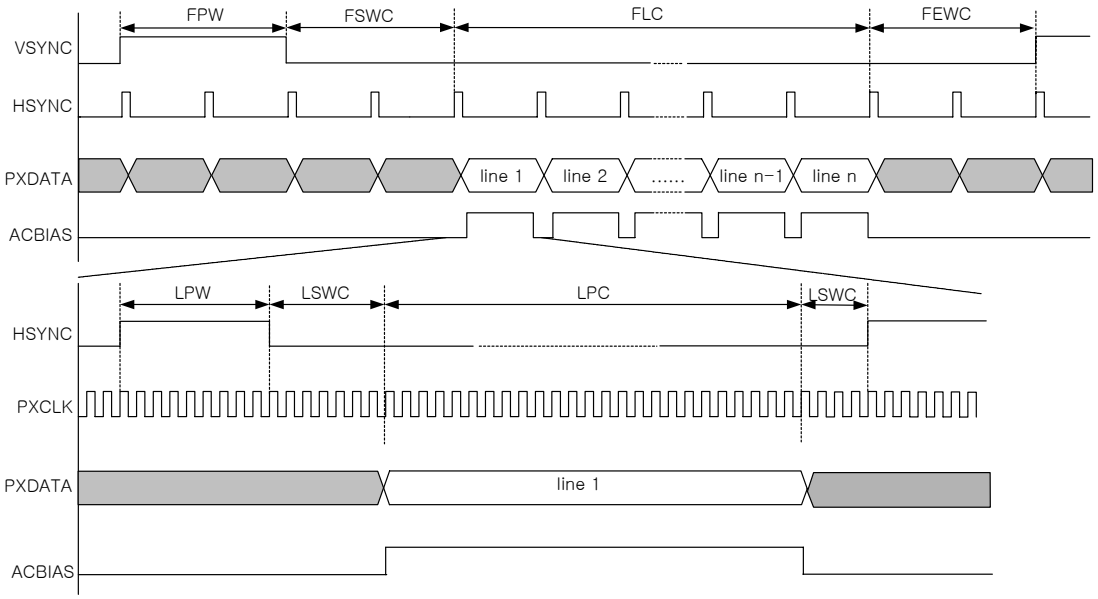


Figure 5.1 Timing Diagram for LCD Controller

The LHS (HSYNC), LVS (VSYNC), LBIAS (ACBIAS, Data Enable) and LPD[17:0] (PXDATA[17:0]) signals are referenced by LCK (PXCLK). Each min and max timing for the output delay are shown in the following figure.

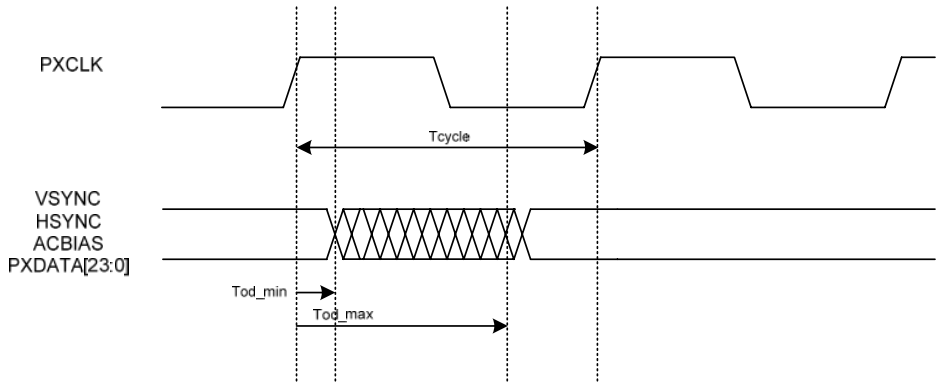


Figure 5.2 Timing Diagram Data Output Referenced to PXCLK

Table 5.17 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
Clock Cycle	T_{CYCLE}	10	-	ns	
Output Delay	T_{OD}	0	TBD	ns	

Table 5.18 I/O Function Name for Corresponding Signal Name

Signal Name	I/O Function Name
VSYNC	L0_LVS, L1_LVS
HSYNC	L0_LHS, L1_LHS
ACBIAS	L0_LDE, L1_LDE
PXDATA[23:0]	L0_LPD[23:0], L1_LPD[23:0]
PXCLK	L0_LCK, L1_LCK

The following figure shows the timing diagram of bus interface to CPU I/F LCD device. The reference clock is used internally and the cycle time is defined as the register value written by software.

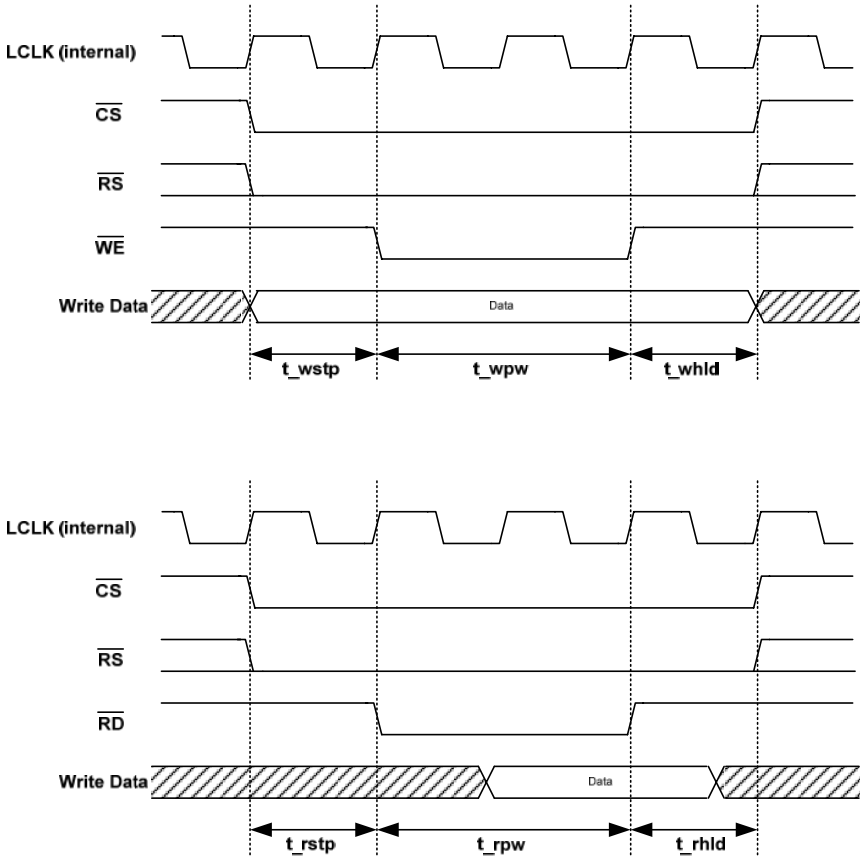


Figure 5.3 Timing Diagram Data Output Referenced to LCDSI

Table 5.19 Timing Parameters for Each Symbols

Parameter	Symbol	Min	Max	Unit	Remark
LCLK Clock Period (LCDSI Clock)	tCLK	TBD		ns	
RD/WE Setup Time Referenced to LCLK	T_rstp	0 * tCLK	7 * tCLK	ns	
RD/WE Pulse Width Referenced to LCLK	T_rpw	1 * tCLK	256 * tCLK	ns	
RD/WE Hold Time Referenced to LCLK	T_rhld	0 * tCLK	7 * tCLK	ns	

Signal Name	I/O Function Name
#CS	LCSN0, LCSN1
#RS	LXA[0]
#RD	LOEN
#WE	LWEN
Write Data[17:0]	LXD[17:0]

5.12 Electrical Characteristics for Camera Interface

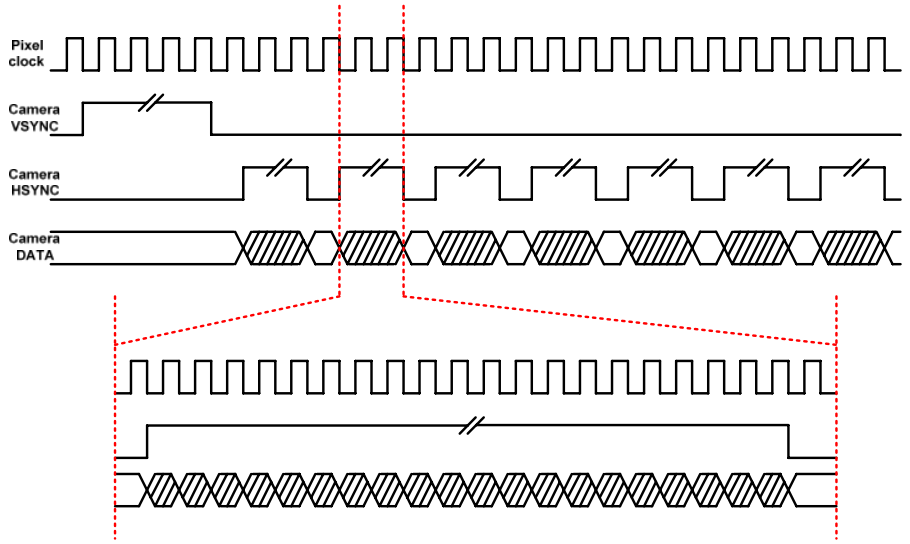


Figure 5.4 Timing Diagram for Camera Interface

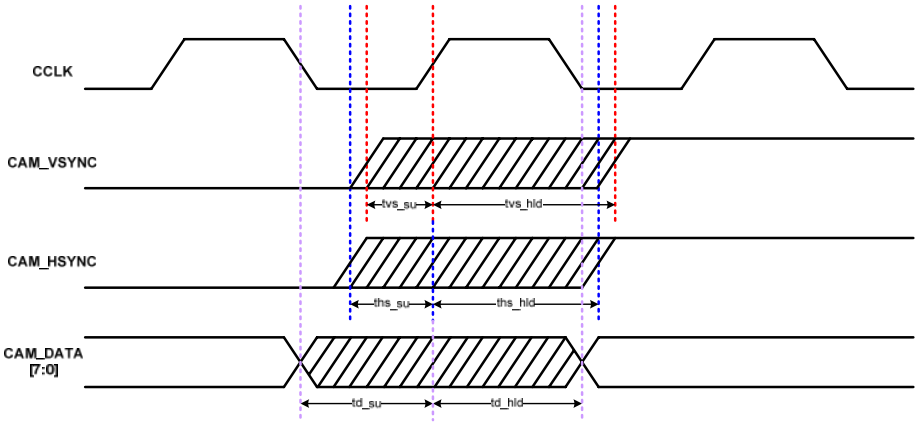


Figure 5.5 Timing Diagram Data Output Referenced to CCLK

Table 5.20 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
Clock Frequency	TCCK		TBD	MHz	
Setup time for CVS(CAM_VSYNC)	Tvs_su	2		ns	
Hold time for CVS(CAM_VSYNC)	Tvs_hld	2		ns	
Setup time for CHS(CAM_HSYNC)	Ths_su	2		ns	
Hold time for CHS(CAM_HSYNC)	Ths_hld	2		ns	
Setup time for CPD[7:0](CAM_DATA)	Td_su	2		ns	
Hold time for CPD[7:0](CAM_DATA)	Td_hld	2		ns	

Table 5.21 I/O Function Name for Corresponding Signal Name

Signal Name	I/O Function Name
CCLK	CCKI
CAM_VSYNC	CVS
CAM_HSYNC	CHS
CAM_DATA[7:0]	CPD[7:0]

5.13 Electrical Characteristics for External Host Interface (EHI)

The EHI has two clock inputs; one is HCLK, which is for the on-chip system bus, the other is ECLK, which is for interface with the external host device. Therefore, interface timing with the external host is only related with ECLK.

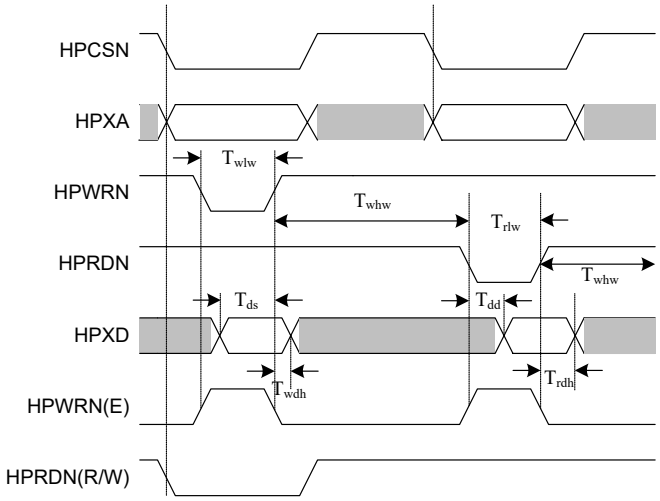


Figure 5.6 EHI Timing Diagram

Symbol	Description	Min.	Max.	Unit
Twlw	Write low width	2TP[18]	-	ns
Twhw	Write high width	3TP	-	ns
Trlw	Read low width	4TP	-	ns
Trhw	Read high width	3TP	-	ns
Tds	Data setup time	10	-	ns
Twdh	Write data hold	5	25ns	ns
Tdd	Data delay time	-	3TP +10ns	-
Trdh	Read data hold	0		ns

18 TP = ECLK period (ns)

5.14 Electrical Characteristics for SD/MMC Controller

The SD/MMC host controller is designed to supports high-speed mode (SD rev.1.10, up to 50 MHz Clock) as well as default speed mode (SD rev.1.01, up to 25 MHz Clock). A user doesn't need to set differently our SD/MMC host controller for mode change between default mode and high speed mode. If you want to change mode to high-speed mode from default mode and vice versa, by using switch-function command (CMD6), the SD/MMC cards are set to such mode. The timing diagram shows the input/output timing criterion referenced to SD/MMC clock.

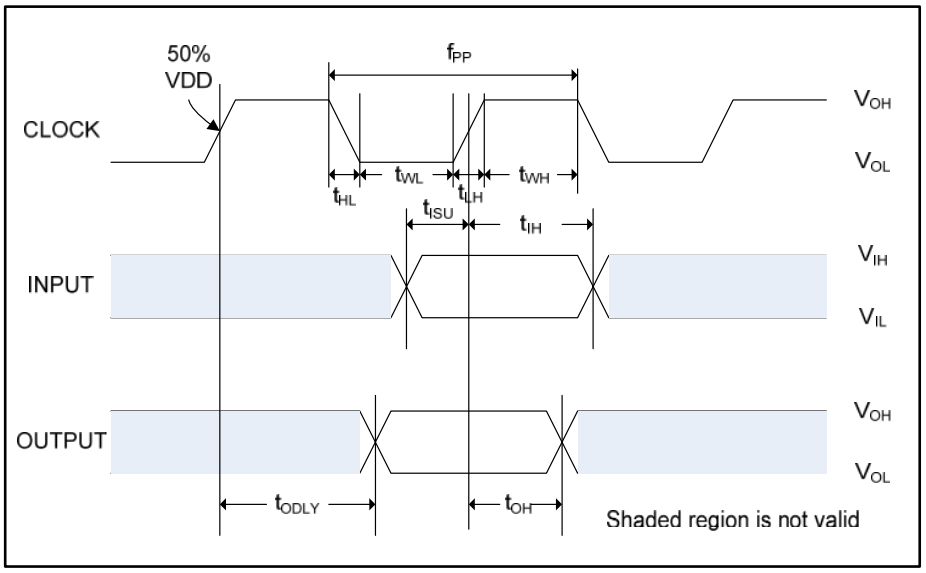


Figure 5.7 Timing Diagram for SD/MMC Controller

Table 5.22 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
Clock frequency Data Transfer Mode	fPP	0	TBD	MHz	Ccard ≤ 30pF
Clock low time	tWL	7		ns	Ccard ≤ 30pF
Clock high time	tWH	7		ns	Ccard ≤ 30pF
Clock rise time	tLH		3	ns	Ccard ≤ 30pF
Clock fall time	tHL		3	ns	Ccard ≤ 30pF
Input set-up time	tISU	6		ns	Ccard ≤ 30pF
Input hold time	tIH	2.5		ns	Ccard ≤ 30pF
Output delay time	tODLY	10		ns	Ccard ≤ 30pF
Output hold time	tOH	2		ns	Ccard ≤ 30pF

5.15 Electrical Characteristics for I2C Controller

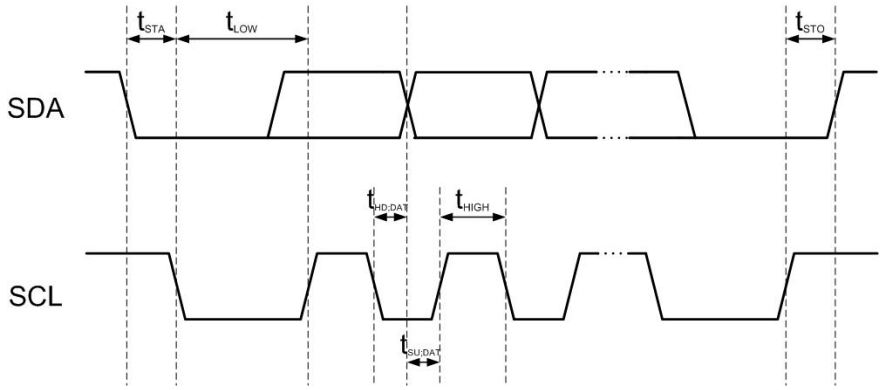


Figure 5.8 Timing Diagram for I2C Controller

Table 5.23 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
SCL clock frequency		0	400	KHz	
Hold time(repeated) START condition	tSTA	0.95	-	us	
Data hold time	tHD:DAT	0.9		us	
Data setup time	tSU:DAT	0.4	-	us	
HIGH period of the SCL clock	tHIGH	0.96	-	us	
LOW period of the SCL clock	tLOW	1.4	-	us	
Setup time for STOP condition	tSTO	1.0	-	us	

5.16 Electrical Characteristics for SPDI/F Transmitter

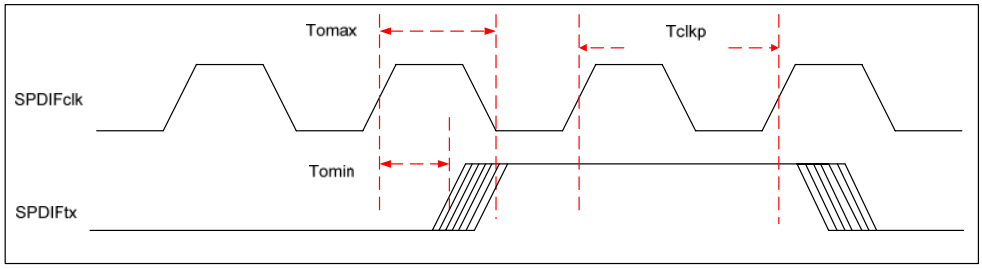


Figure 5.9 Timing Diagram for SPDI/F Transmitter

Table 5.24 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
SPDIFclk Clock Cycle Time	Tclkp	110		ns	
SPDIFclk Data Output Time Referenced to SPDIFclk	Tomin/Tomax	1	10	ns	CL = 50pF

5.17 Electrical Characteristics for DAI(I2S)

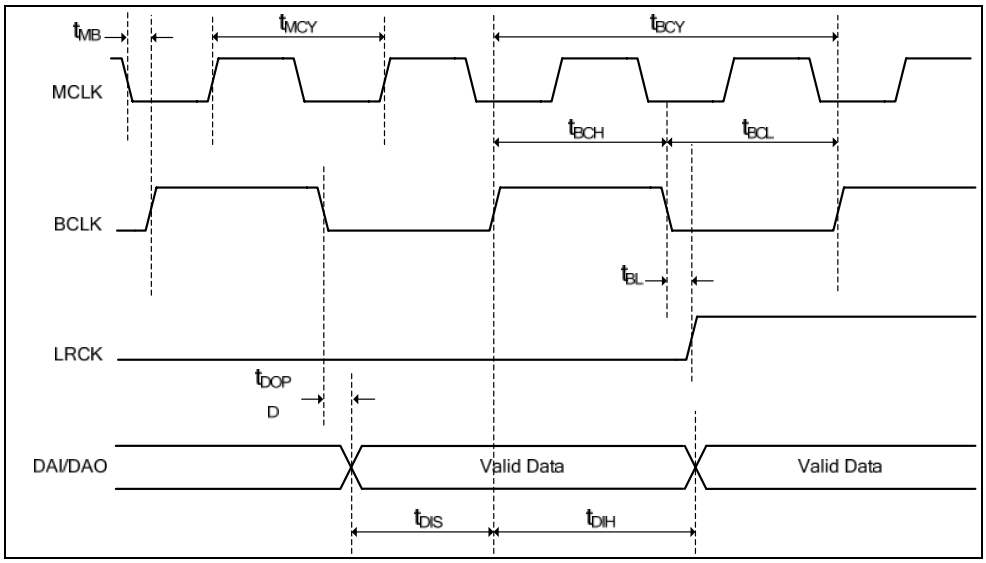


Figure 5.10 Timing Diagram for DAI (receiver)

Test Conditions
MODE = I2S, fs = 48KHz, MCLK = 256fs, BCLK = 64fs, (Polatity: DAMR[16] = '0', DAMR[3] = '0')

Table 5.25 Timing for DAI

Parameter	Symbol	Min	Typ	Max	Unit	Remark
MCLK cycle time	tMCY	19.40	81.40		ns	
BCLK cycle time	tBCY	4 * tMCY	4 * tMCY		ns	
BCLK pulse width high	tBCH	39	163		ns	
BCLK pulse width low	tBCL	38	162		ns	
MCLK to BCLK	tMB	-3	3		ns	
BCLK to LRCK	tBL	-3	3		ns	
DAI setup time to BCLK rising edge	tDIS	1	1		ns	
DAI hold time from BCLK rising edge	tDIH	1	1		ns	
DAO Output Timing Referenced to BCLK	tDOPD			1	ns	

5.18 Electrical Characteristics for Nand Flash Controller

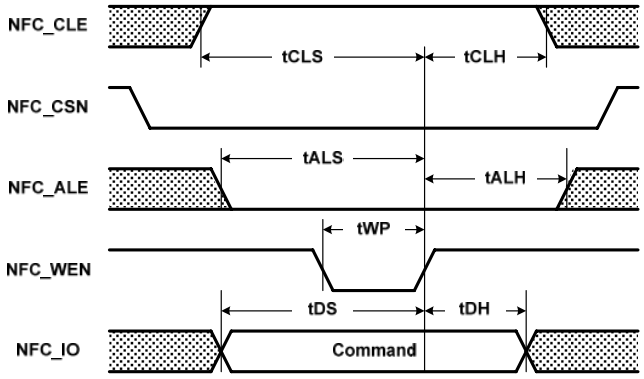


Figure 5.11 Timing Diagram for Command Latch Enable Cycle

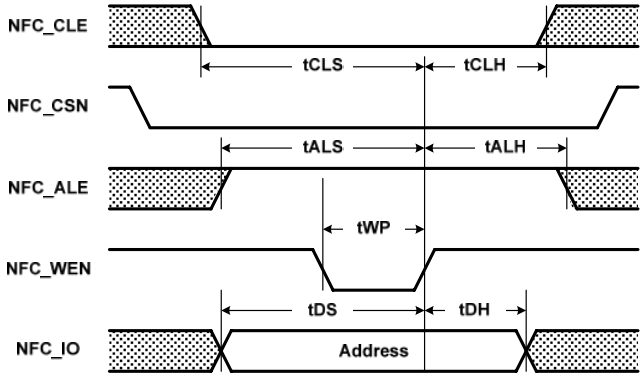


Figure 5.12 Timing Diagram for Single Address Latch Cycle

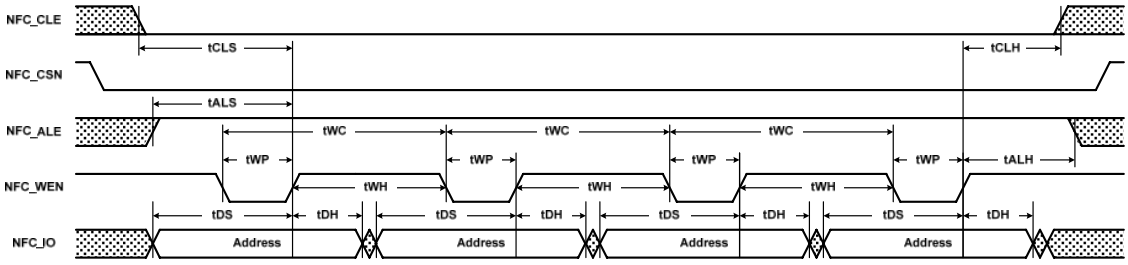


Figure 5.13 Timing Diagram for Linear Address Latch Cycle

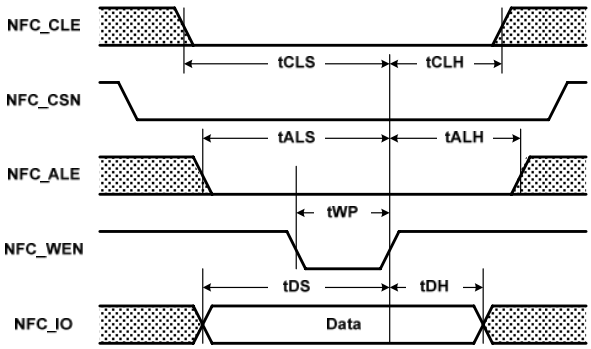


Figure 5.14 Timing Diagram for Single Data Write Cycle

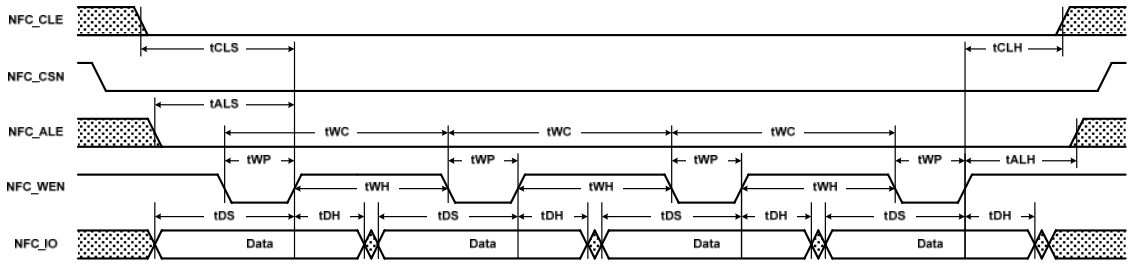


Figure 5.15 Timing Diagram for Linear Data Write Cycle

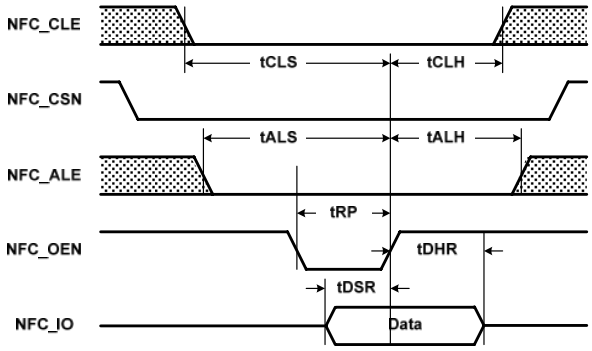


Figure 5.16 Timing Diagram for Single Data Read Cycle

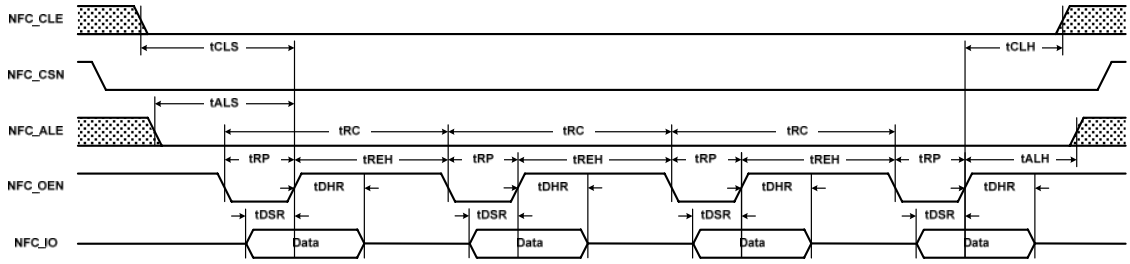


Figure 5.17 Timing Diagram for Linear Data Read Cycle

Table 5.26 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit
Clock Period	tHCLK	6		ns
CLE Set-Up Time	tCLS	(STP + PW) x tHCLK + 1.0	(STP + PW) x tHCLK + 2	ns
CLE Hold Time	tCLH	HLD x tHCLK – 2.0	HLD x tHCLK – 1.0	ns
WEN Pulse Width	tWP	PW x tHCLK	PW x tHCLK	ns
WEN High Hold Time	tWH	(STP + HLD) x tHCLK	(STP + HLD) x tHCLK	ns
Write Cycle Time	tWC	(STP + PW + HLD) x tHCLK	(STP + PW + HLD) x tHCLK	ns
OEN Pulse Width	tRP	PW x tHCLK	PW x tHCLK	ns
OEN High Hold Time	tREH	(STP + HLD) x tHCLK	(STP + HLD) x tHCLK	ns
Read Cycle Time	tRC	(STP + PW + HLD) x tHCLK	(STP + PW + HLD) x tHCLK	ns
ALE Set-Up Time	tALS	(STP + PW) x tHCLK – 1.00	(STP + PW) x tHCLK + 2.00	ns
ALE Hold Time	tALH	HLD x tHCLK – 2.00	HLD x tHCLK + 1.00	ns
Data Set-Up Time	tDS	(STP + PW) x tHCLK – 7.00	(STP + PW) x tHCLK – 1.00	ns
Data Hold Time	tDH	HLD x tHCLK – 1.00	HLD x tHCLK + 1.00	ns
Data Set-Up Time in READ	tDSR	5.00	15.0	ns
Data Hold Time in READ	tDHR	0	0	ns

Table 5.27 I/O Function Name for Corresponding Signal Name

Signal Name	I/O Function Name
NFC_CSN	NAND_CSN0, NAND_CSN1
NFC_ALE	NAND_ALE
NFC_CLE	NAND_CLE
NFC_OEN	NAND_OEN
NFC_WEN	NAND_WEN
NFC_IO[15:0]	NANDXD[15:0]

5.19 Electrical Characteristics for UART Controller

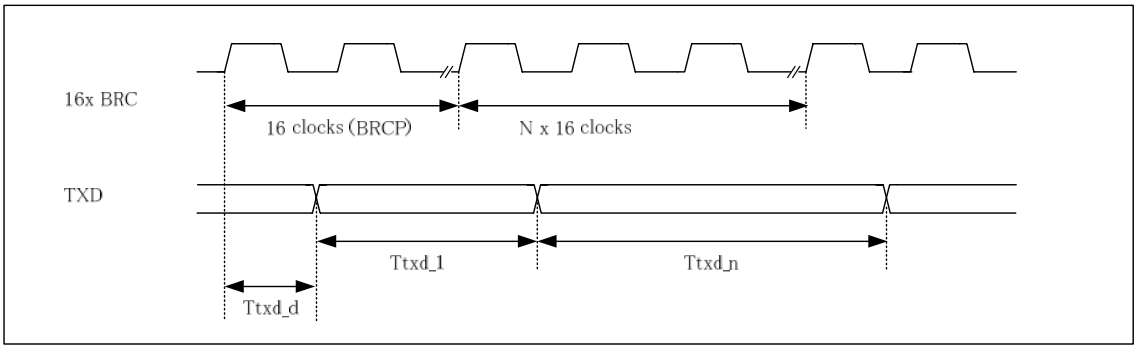


Figure 5.18 Timing Diagram for TXD

Table 5.28 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
Pulse duration of 1bit TXD	Ttxd_1	BRCP -15	BRCP +15	ns	3.3V
Pulse duration of nbit TXD	Ttxd_n	N x BRCP -15	N x BRCP + 15	ns	3.3V
TXD output delay time	Ttxd_d	0.5	15	ns	3.3V

- BRC : Baud-Rate Clock
- BRCP : Baud-Rate Clock Period
- CL : 71pF

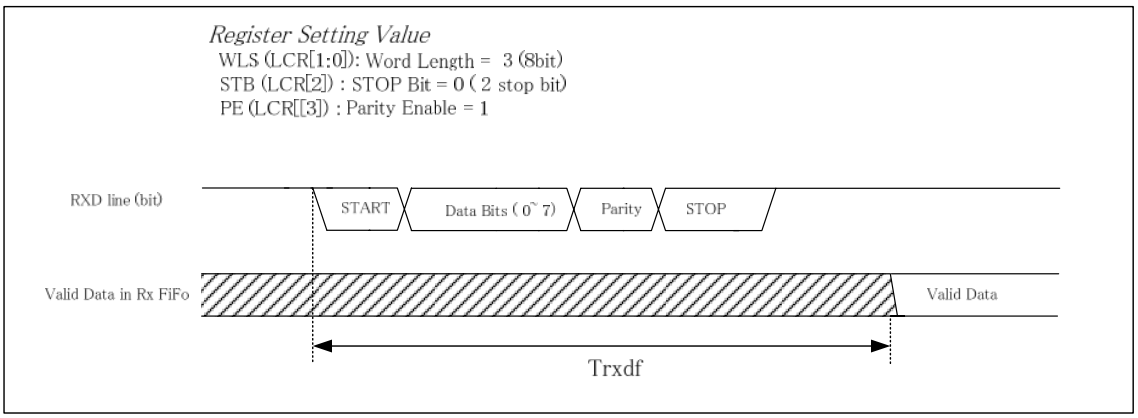


Figure 5.19 Timing Diagram for RXD

Table 5.29 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
RXD Start to Rx FiFo.	Trxdf	10.5 x BRCP	11 x BRCP	ns	3.3V

- BRC : Baud-Rate Clock
- BRCP : Baud-Rate Clock Period
- CL : 71pF

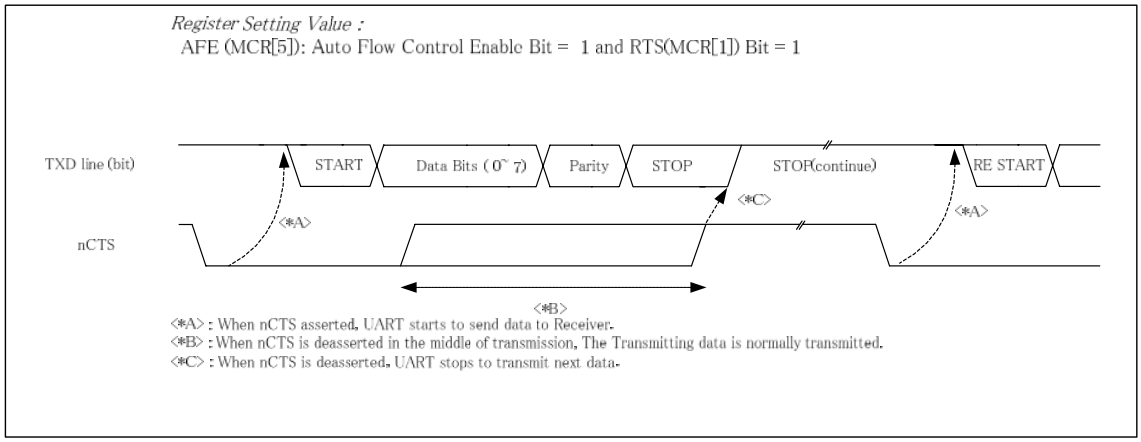


Figure 5.20 Timing Diagram for TX Operation with H/W Flow Control

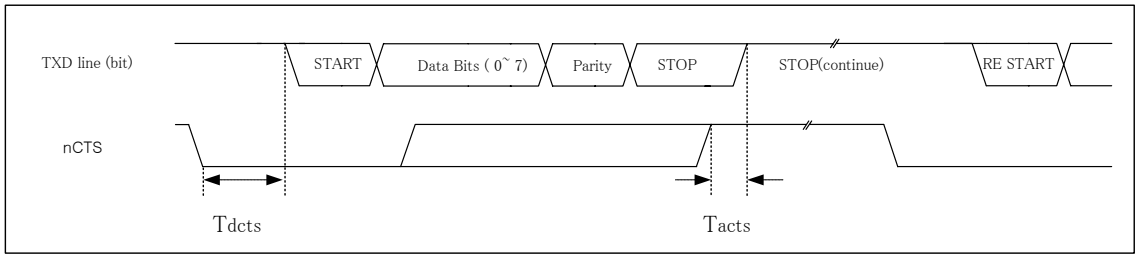


Figure 5.21 Timing Diagram for nCTS Timing Diagram

Table 5.30 Timing Parameters for Each Symbol

Parameter	Symbol	Min	Max	Unit	Remark
Deasserted nCTS to Tx Start	Tdcts	-	BRCP	ns	3.3V
Deasserted nCTS to Tx Stop :to stop next transmission(setup time)	Tacts	4 x BRCP/16	-	ns	3.3V

- BRC : Baud-Rate Clock , BRCP : Baud-Rate Clock Period , CL : 71pF

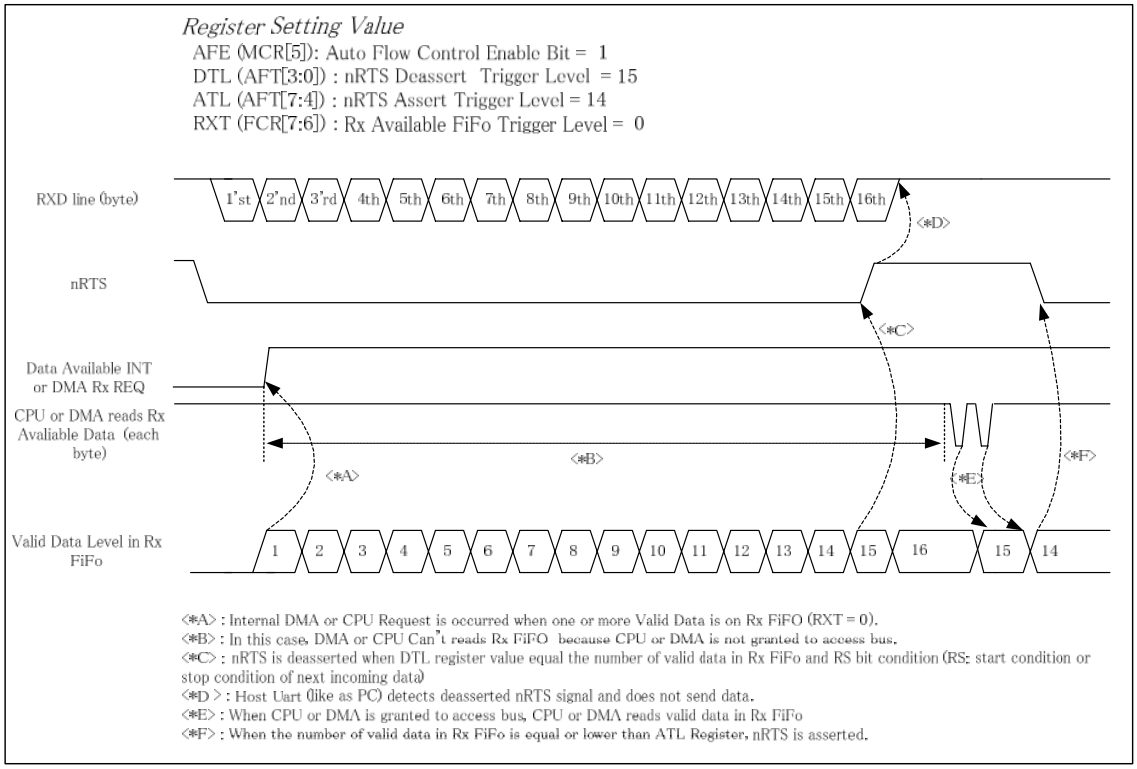


Figure 5.22 Timing Diagram for RX Operation with H/W Flow Control

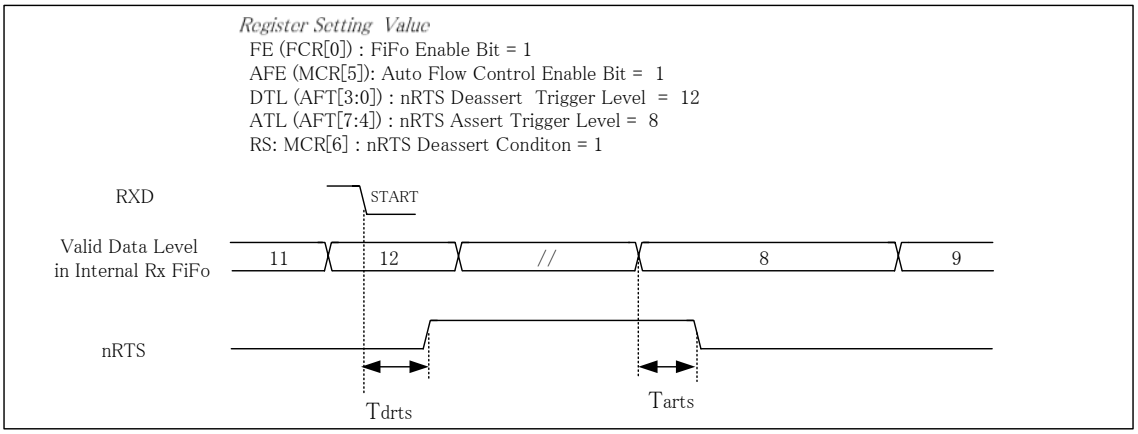


Figure 5.23 Timing Diagram for nRTS Timing Diagram

Table 5.31 Timing Parameters for Each Symbols

Parameter	Symbol	Min	Max	Unit	Remark
DTL(and RXD start condition) to deasserted nRTS	Tdrts	-	BRCP	ns	3.3V
ATL to asserted nRTS	Tarts	-	BRCP/16 + 8	ns	3.3V

- BRC : Baud-Rate Clock , BRCP : Baud-Rate Clock Period , CL : 71pF

5.20 Electrical Characteristics for DDR

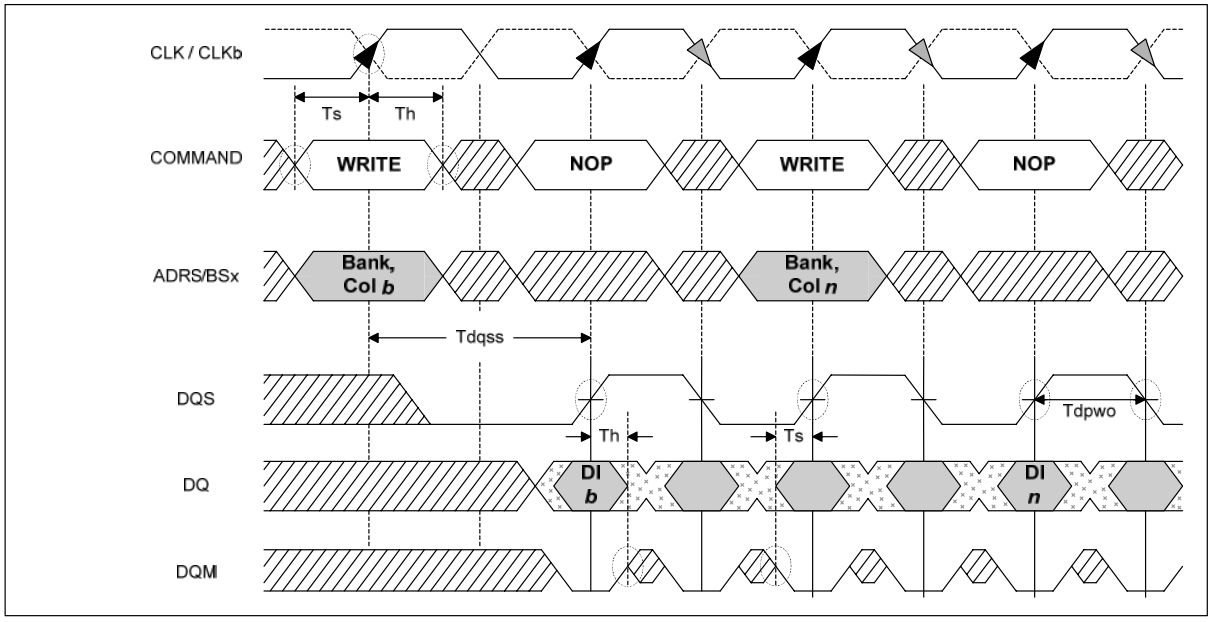


Figure 5.24 Write Cycle Timing

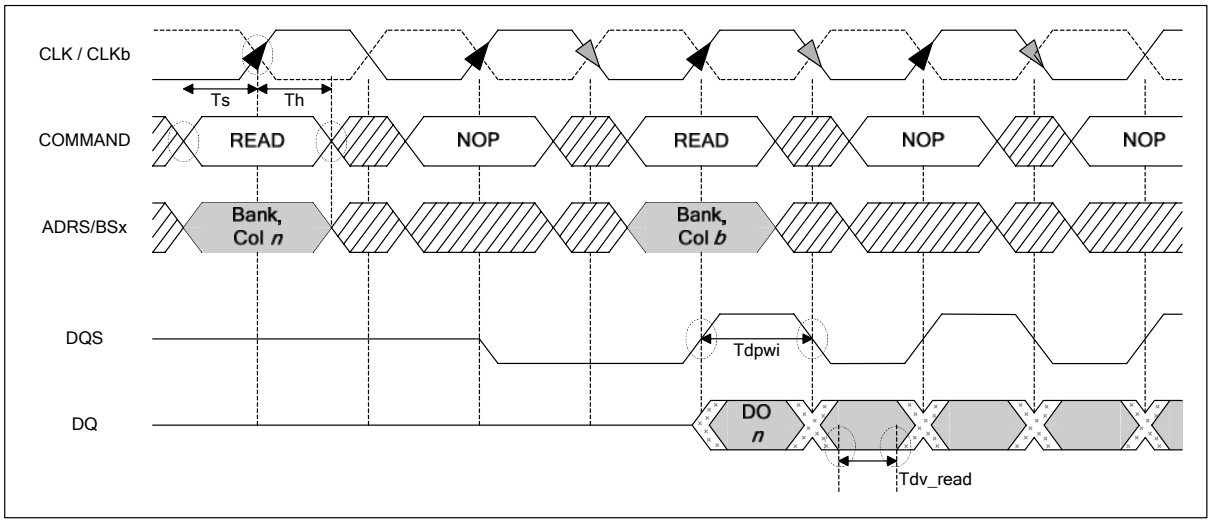


Figure 5.25 Read Cycle Timing

Table 5.32 DDR Interface Timing Parameters

S.No	Parameter	Notation	Min (ns)	Max (ns)
1	Clk Period	tCK	TBD	-
2	Clk High level width	tCH	TBD	-
3	Clk Low level width	tCL	TBD	-
4	RASb output setup time with regard to (w.r.t.) clock	Ts	0.6	-
5	CASb output setup time with regard to clock	Ts	0.6	-
6	WEb output setup time with regard to clock	Ts	0.6	-
7	CKE output setup time with regard to clock	Ts	0.6	-
8	Addr output setup time with regard to clock	Ts	0.6	-
9	BA output setup time with regard to clock	Ts	0.6	-
10	RASb output hold time with regard to clock	Th	0.6	-
11	CASb output hold time with regard to clock	Th	0.6	-
12	WEb output hold time with regard to clock	Th	0.6	-
13	CKE output hold time with regard to clock	Th	0.6	-
14	Addr output hold time with regard to clock	Th	0.6	-
15	BA output hold time with regard to clock	Th	0.6	-
16	DQS output pulse width	Tdpwo	TBD	-
17	DQ output setup time with regard to DQS	Ts	0.105	-
18	DQ output hold time with regard to DQS	Th	0.105	-
19	DQM output setup time with regard to DQS	Ts	0.105	-
20	DQM output hold time with regard to DQS	Th	0.105	-
21	Required input data window for reads (DQ)	Tdv_read	0.144	-
22	Required input DQS pulse width (DQS)	Tdpwi	TBD	-